CPC5622-EVAL-600R
LITELINK™ III Evaluation Board
User's Guide

1. Introduction

Thank you for using IXYS IC Division's CPC5622-EVAL-600R evaluation board. The evaluation board ships with the CPC5622A LITELINK III and CPC5712U Voltage Monitor to demonstrate the functionality of a PSTN terminating two-wire interface that provides both the analog voice transmission and signaling functions. The analog interface is configured to provide a 600Ω resistive AC impedance with 0dB gain in both the transmit and receive directions. While the CPC5622A provides the hook-switch and ringing detect signaling functions, the CPC5712U is utilized to monitor and detect changes in the DC line voltage to determine loop status and signaling information sent by the network. Loop status is given by the logic level outputs of the three CPC5712U on-board detectors indicating Loop Presence, Line In Use, and Loop Polarity.

CPC5622-EVAL-600R evaluation board top and bottom views are shown in the following illustrations.

Figure 1. Evaluation Board Top View

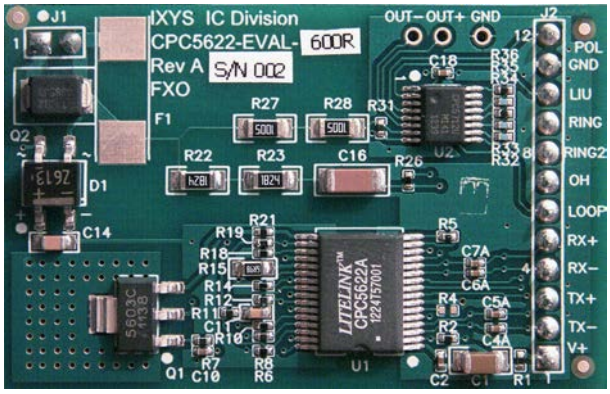
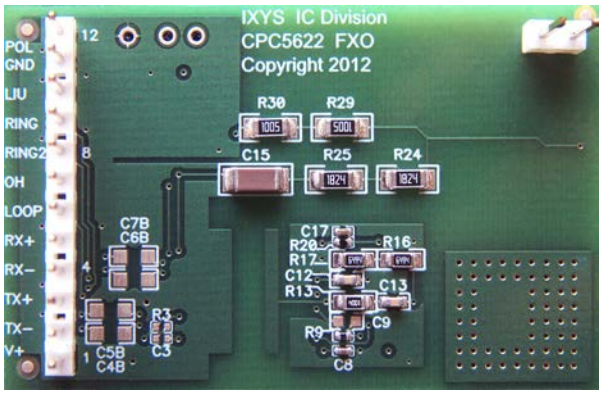


Figure 2. Evaluation Board Bottom View



The printed-circuit board used for the CPC5622-EVAL-600R evaluation board is a multi-purpose board that facilitates prototyping of many PSTN line interface configurations by simple component changes. Specific evaluation board models provided by IXYS IC Division can be identified by the label appended to the core part number "CPC5622-EVAL-". The suffix label "600R" as shown in Figure 1 for this model indicates the two-wire AC input impedance is 600Ω. For the 600R model, the transmit and receive gains are 0dB.

- 600R = 600Ω resistive AC termination with 0dB transmit and receive gains.

In addition to the model identification label some boards may have a second label located just below the evaluation board part number indicating the evaluation board's serial number.

2. Setup and Using the Evaluation Board

This section describes setting up the CPC5622-EVAL-600R Evaluation Board prior to use.

2.1 Connections

The CPC5622-EVAL-600R evaluation board uses two 100 mil (2.54 mm) pitch pin headers, J1 and J2, for the input and output connections. IXYS IC recommends constructing header jumpers to bring the connections out to your development or test platform. Connector J1, the two-position pin header, provides access to the PSTN loop connections while J2, the 12-position pin header, provides access for the low voltage side power, logic control, logic-level loop status detector outputs and the analog transmit and receive voice paths.

Table 1: Telephone Network Access Connector - J1

Pin	Silk Screen	Schematic Name	Use
1	1	RING	Connect to the Ring (B) lead of the telephone network or a loop simulator.
2		TIP	Connect to the Tip (A) lead of the telephone network or a loop simulator.

Table 2: Low Voltage Side Power and Signal Connector - J2

Pin	Silk Screen	Schematic Name	Use
1	V+	VCC	Power input: +3.3 V_{DC} or +5 V_{DC}
2	TX-	TX-_IN	Inverting analog input to the LITELINK
3	TX+	TX+_IN	Non-inverting analog input to the LITELINK
4	RX-	RX-_OUT	Negative analog output from LITELINK
5	RX+	RX+_OUT	Positive analog output from LITELINK
6	LOOP	LOOP	Loop Presence detector output
7	OH	OH*	Hook switch control. Off-Hook: OH* = 0, On-Hook: OH* = 1
8	RING2	RING2*	Full-wave ringing detector output
9	RING	RING*	Half-wave ringing detector output
10	LIU	LIU*	Line In Use detector output
11	GND		Low voltage side ground
12	POL	POLARITY	Polarity Detector output

NOTE: For clarity and consistency with the schematic, the schematic names will be used from this point forward throughout the text.

2.2 Using the Evaluation Board

Follow these guidelines for productive use of the LITELINK evaluation board:

- Evaluation board circuit components are sensitive to electrostatic discharge (ESD). Use normal ESD precautions when working with the LITELINK III evaluation board.
- Make all low voltage side connections (J2) to the board before applying power to VCC.
  Tip and Ring connections at J1 can be made at any time before or after VCC power is applied.
- OH* should be open or tied to the VCC input power pin during power up and held for 50us after power up.
- Pulling OH* low will cause the CPC5622 to go off-hook and returning OH* high will cause the unit to go back on-hook.
- Analog transmission in both the transmit path and the receive path is enabled while off-hook. When on-hook, only the receive path is enabled.
- For proper off-hook operation, the Tip and Ring interface must be appropriately biased and terminated.
- The CPC5622 RING* and RING2* ringing detectors are only active while on-hook.
- The CPC5712U line voltage and polarity detectors are active in both the on-hook and off-hook states.

3. Functional Description

The CPC5622-EVAL-600R provides the analog interface and signaling functions necessary to implement a PSTN two-wire terminating device for voice and data applications such as PBX FXO, cordless telephones, FAX machines, set top boxes, card readers, ATMs, and modems. Analog gains in both the transmit and receive paths for the 600R evaluation board are set to 0dB with the impedance of the two-wire interface configured for 600 ohms resistive. These analog functions are provided by the CPC5622A Phone Line Interface integrated circuit. Additionally, the CPC5622A provides the basic signaling functions of loop closure / loop open and ringing detect that are required for a two-wire, current sink, loop start interface. It is important to note that it is not within the scope of this document to provide complete behavioral descriptions of the CPC5622A or the CPC5712U functions as this information is covered in the data sheets and the appropriate application notes.

Basic signaling functions for a loop start, current sink interface are loop closure (Off-Hook), loop open (On-Hook) and ringing detect. Loop closure / open is provided by the hook switch control function with ringing detect provided by the Snoop input circuit and the internal ringing detector. Additional loop voltage detectors used to determine the line status are provided by the CPC5712U Voltage Monitor with Detectors integrated circuit. Line condition status provided by the CPC5712U voltage detectors are: Line In Use (LIU), Loop battery presence (LOOP), and Polarity. While these detectors are not required for the most basic applications, they are required by the majority and are therefor provided on the evaluation board. Access to the analog paths and the detector functions is provided by the two connectors J1 and J2. Tip and Ring loop access is provided by J1 while J2 provides access to the low voltage side (SELV) power and signals.

This evaluation board differs from previous generation evaluation boards by incorporating a common mode noise cancellation circuit that improves longitudinal balance and common mode rejection across the voice band spectrum. This is accomplished by using a small capacitance from shapes on the printed circuit board (PCB) and modifications to the recommended passive components values that set the analog transmission parameters. Details in the construction of the PCB capacitor are provided in the evaluation board's printed circuit board design files available on line.

3.1 Connector J1 - Tip and Ring

Connector J1, the two-pin header, provides access to the Tip and Ring (T/R) terminals of the evaluation board. The Ring lead is located on pin 1 of the connector and pin 2 is the Tip lead. Although the board's layout is designed for lightning and power cross surge testing, the connector and it's 25 mil square pins are not rated for the peak voltages or currents specified in the safety regulations. It is suggested the connector be removed and lead wires be soldered to the board when performing these tests.

3.2 Connector J2 - Low Voltage Side Interface

Providing access to the low voltage side analog and digital interface is connector J2, a single row 12-pin header connector with 25 mil square pins on 100 mil centers. Due to space limitations, the silkscreen pin names where modified slightly from the net names shown on the schematic. These naming differences are shown in Table 1 and Table 2 on Page 2.

Pin 1: VCC

Power pin for the low voltage (SELV) side circuits. Apply a nominal $3.3V_{DC}$ or $5V_{DC}$ with respect to the ground (GND) connection at Pin 11.

Pin 2: TX-_IN

Pin 3: TX+_IN

Pins 2 and 3 are the analog voice negative (TX-) and positive (TX+) differential inputs for the transmit path (SELV to T/R). The maximum signal applied to these input pins is 0dBm. (This is 0.548Vp on each input.) For applications where the analog source is single ended, short one of the input pins to ground and apply the analog signal to the other input. Typically, TX- is shorted to ground and the signal is applied to TX+. For single ended applications, the maximum input signal is still 0dBm. (This is 1.095Vp.)

Pin 4: RX-_OUT

Pin 5: RX+_OUT

Pins 4 and 5 are the analog voice negative (RX-) and positive (RX+) differential outputs for the receive path (T/R to SELV). The maximum output signal by these pins is 0dBm. This is 0.548Vp on each output.
For single ended receive applications, connect one of the output pins to the receiver input pin and leave the other output open. This will result in a receive path loss of 6dB.

Pin 6: LOOP

This is a logic level output indicating the presence of loop battery feed from the network. For tip to ring voltages greater than approximately $+/-5V_{DC}$ the detector will output a logic high (LOOP = 1) and for T/R voltages less than approximately $+/-3V_{DC}$ the detector will output a logic low (LOOP = 0). The LOOP detector is polarity insensitive.

Pin 7: OH*

OH* is an active low, TTL compatible, logic level input used to control the hook switch function of the T/R network interface. Applying a logic low (OH* = 0) at this pin will enable the gyrator located on the line side causing DC current to flow. This is commonly referred to as the "Off-Hook" state. The gyrator, an electronic inductor, has a low impedance at DC but a high impedance in the voice band allowing the two-wire interface to draw DC loop current without loading the AC termination. An On-Hook state occurs when OH* = 1 and loop current ceases.

The OH* net is connected to the $\overline{OH}$ input at pin 8 of the CPC5622A. The CPC5622A requires this input to be left open or pulled high to VCC during power up and for a minimum duration of 50us following power up. An internal pull-up resistor at the $\overline{OH}$ input provides the required logic high when the input is left open.

Pin 8: RING2*

This is the full wave ringing detect output $\overline{\text{RING2}}$ of the CPC5622A. The output signal will be a logic low whenever the incoming ringing signal exceeds the threshold of the CPC5622A internal voltage detector. With ringing applied, the output will be a series of negative pulses at twice the frequency of the ringing signal. The width of the negative pulses will be a function of the ringing signal amplitude.

Pin 9: RING*

This is the half-wave ringing detect output $\overline{\text{RING}}$ of the CPC5622A. The description of this output signal is similar to $\overline{\text{RING2}}$ above but the output pulses will have the same frequency as the incoming ringing signal.

Pin 10: LIU*

LIU* is a logic level output indicating an off-hook by another device on tip and ring whenever the CPC5622A is on-hook. With a T/R voltage less than approximately +/-14V_{DC} an Off-Hook indication (LIU* = 0) is output. For tip to ring voltages greater than approximately +/-17V_{DC} the detector will output a logic high (LIU* = 1). As with the LOOP detector, the LIU* detector is polarity insensitive.

Declaring the line to be Off-Hook when LIU* = 0 is only valid when loop battery is present, LOOP = 1.

Pin 11: GND

This is the low voltage side (SELV) ground. All low voltage side signals are referenced from this net. The tip and ring voltages as well as the line side signals are NOT referenced from the low voltage side ground.

Pin 12: POLARITY

POLARITY is a logic level output that indicates the polarity of the battery feed on tip and ring. POLARITY = 1 for normal battery when the Tip is more positive than the Ring. When the battery polarity is reversed causing Ring to be more positive than Tip, the detector will output POLARITY = 0. The POLARITY detector nominal thresholds are set at 2V_{DC}.

The POLARITY detector does not change state until the increasing line voltage potential passes through the switching point. This ensures the POLARITY detector output will remain stable at it's last state if battery feed from the network is lost.

3.3 Tip to Ring Conditioning

When using the CPC5622 evaluation board, the tip to ring interface must be properly configured with DC bias for off-hook AC transmission as the CPC5622 line side circuitry derives it's operating power from the network. In addition, the CPC5622 must have a tip to ring AC termination impedance equal to the evaluation board's two-wire input impedance for correct analog transmission performance. The required tip to ring termination impedance for the CPC5622-EVAL-600R evaluation board is 600Ω.

For basic functional testing, the tip and ring may be connected to an external PSTN line. While these lines provide DC bias and an acceptable AC termination for access to the network, they are not suitable for lab quality measurements.

General purpose evaluations can be made using a phone line simulator, also known as a Central Office (CO) line simulator, to source the DC loop current and to provide a reasonable AC impedance. Using a line simulator rather than an external PSTN line eliminates the variable AC impedance and DC feed characteristics caused by the outside cable plant.

Lab quality measurements are typically made using a DC feed circuit conforming to industry standards and test equipment specific for voice quality testing.

3.4 Analog Transmission

The UG-CPC5622-EVAL-600R evaluation board supports full duplex analog voice transmission while off-hook and receive transmission only when on-hook. The nominal gains for all of these transmission paths is 0dB.

3.5 Loop Status Detectors

In addition to the basic ringing detector provided by the CPC5622A, this evaluation board includes additional detectors to determine the status of the loop. Many telephony products need to know the line's condition to function properly. For instance, an automated calling out device would need to know if the line is available or is currently being used by another piece of equipment while another type of product may need to know if it is about to receive a Caller-ID (CID) transmission. These and other conditions can be derived by monitoring the Tip to Ring voltage and

polarity. This functionality is provided by the compact CPC5712U Voltage Monitor that uses high value resistors to bridge the barrier and only five small resistors to set the voltage detectors switching point thresholds and hystereses.

Three voltage detector outputs provide the information necessary to determine the loop's status. They are: 1) LOOP; 2) LIU*; and 3) POLARITY. The loop status can be determined by examining the state of the detectors.

For example, equipment such as satellite set top boxes and security systems that automatically dial out need to know if the line is attached to the network (loop battery present), and if the line is available for use (no off-hook by another device or a phone). To make this determination, the logical levels of the LOOP and LIU* signals need to be considered.

Because LOOP = 0 indicates there is no battery feed from the network, the line is not available for service and the LIU* output has no meaning. With LOOP = 1, battery feed from the network is present and the LIU* output is used to determine the availability of the line. With LIU* = 0, another device on the line is off-hook and again, the line is not available. Only when LOOP = 1 AND LIU* = 1 is the line available.

3.6 PCB Capacitor and Noise Cancellation Synopsis

This evaluation board addresses a noise issue reported by customers using ungrounded two-prong AC switching power supplies. Ungrounded power supplies generate a common mode voltage on the low voltage side of the device that has frequency components consisting of the power line fundamental, harmonics of the power line frequency, and power supply switching frequencies with harmonics.

A low cost solution is presented that uses the small capacitance from copper shapes on the printed circuit board to insert an inverted phase noise current into a summing amplifier to resolve the transmit path noise issue and manipulation of existing feedback loops to solve the receive path noise issue.

Above the LITELINK symbol on the schematic shown in Figure 3 on Page 8 is a capacitor labeled C_PCB. This very small capacitor of approximately 60 - 85 fF is constructed from PCB copper shapes to couple the common mode noise from the low voltage side into LITELINK's transmit path at the NTS node on pin 26. NTS is an inverting input of an amplifier whose output is located at node NTF on pin 26. Using this amplifier's input as a summing node for the noise, the common mode conversion in the transmit path is greatly reduced. This performance improvement is easily verified by the Longitudinal Balance measurement.

Enhancing the common mode rejection in the transmit path greatly reduces the noise power output onto tip and ring. This provides the mechanism to improve the common mode noise conversion in the receive path. In practice, normal full duplex voice transmission onto tip and ring utilizes a cancellation circuit, commonly referred to as a "transhybrid" circuit, to reduce the power level of the transmit signal being returned to the talker via the receive path. This returned signal is ofttimes referred to as the reflected signal. Transhybrid cancellation circuits are generally implemented using the summing node of an amplifier to null out the reflected signal. Perfect cancellation occurs when the currents of the reflected signal in the receive path and the transmit signal from the transmit path into the summing node have equal magnitude and are 180° apart. In this type of circuit configuration when one signal into the summing node is missing, the other signal is passed through the amplifier and continues through the receive path.

The noise cancellation circuit for the receive path takes advantage of this behavior. With very little of the transmit noise remaining in the signal output onto tip and ring, the noise generated in the transmit path is passed through the transhybrid cancellation circuit and continues through the receive path. When this noise signal combines with the common mode conversion noise generated by the receive path, the two noise signals effectively cancel each other out resulting in a clean receive transmission path. This is due to the noise signals being out of phase with each other and the original transmit noise signal being properly scaled to match the magnitude of the generated receive path noise.

3.7 Stuffing Options

CPC5622-EVAL-600R Evaluation Boards can be used to evaluate LITELINK III circuits connected to virtually any type of host equipment having an analog interface with many types of telephone networks. This flexibility will often require changes to the components in the circuit.

4. Compatibility with the CPC5620A and CPC5621A

The CPC5622-EVAL-600R evaluation board is compatible with the CPC5620A and CPC5621A LITELINKs.

The $\overline{\text{RING2}}$ output at pin 10 of the CPC5622A is the $\overline{\text{CID}}$ input for both of the CPC5620A and CPC5621A devices. This input is used to switch between the on-hook receive transmission function used for CID reception and the ringing detector. The CPC5622A has both these functions enabled concurrently while on-hook.

The CPC5620A outputs a half-wave ringing detect signal on pin 9, the $\overline{\text{RING}}$ output, while the CPC5621A outputs a full-wave ringing detect signal.

Converting the evaluation board over for the CPC5620A or CPC5621A is simply a matter of swapping the LITELINK devices and re-purposing pin 8 of the evaluation board.

5. CPC5622-EVAL-600R Design

Figure 3. LITELINK CPC5622A Schematic

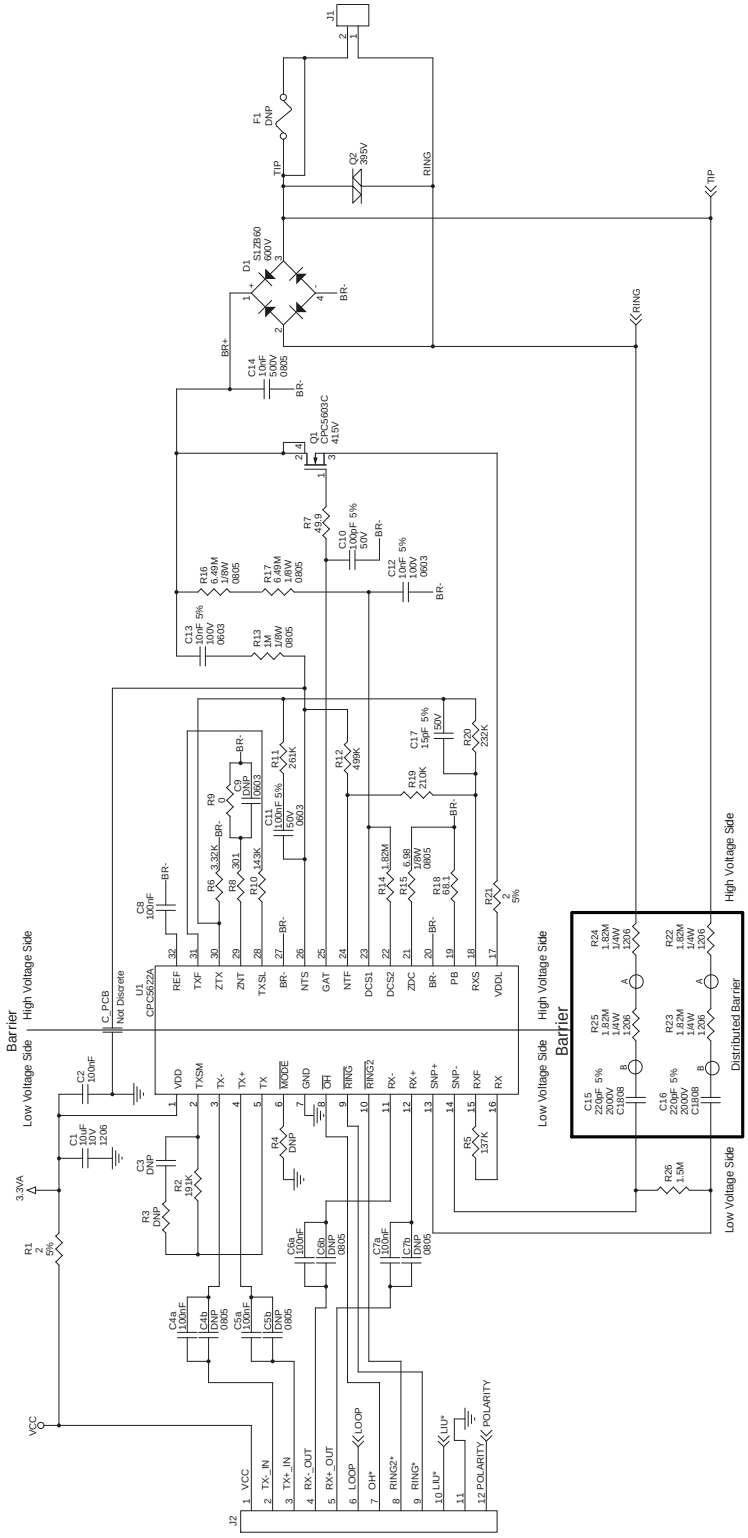
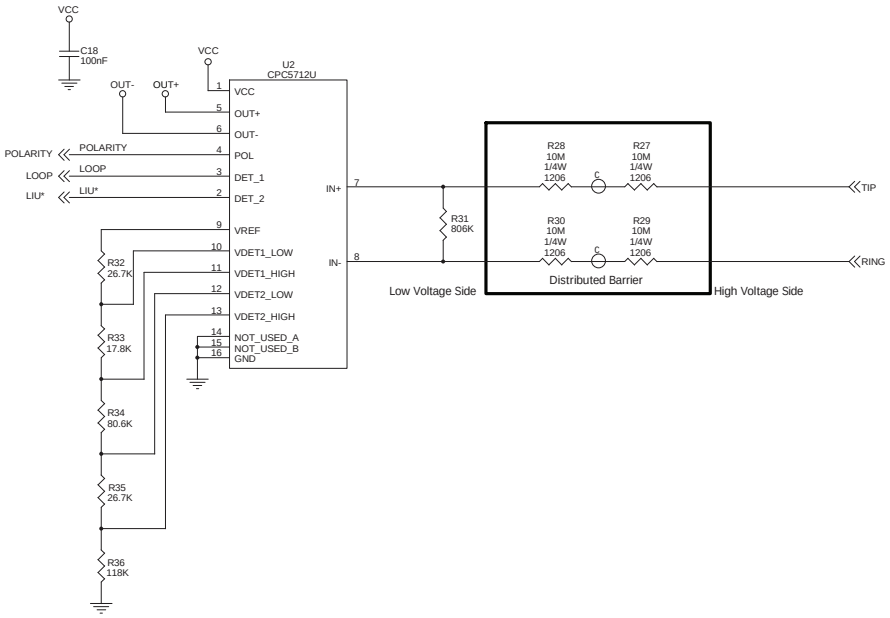


Figure 4. CPC5712U Line Detectors Schematic



5.1 Printed Circuit Board Component Placement

The diagrams below are provided as a quick reference to locate the components.

Figure 5. Top Side Components

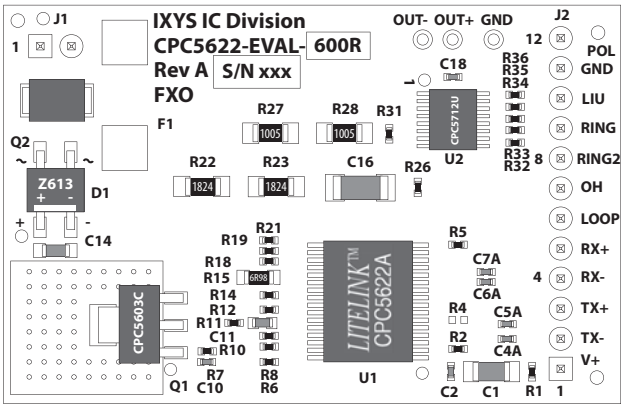
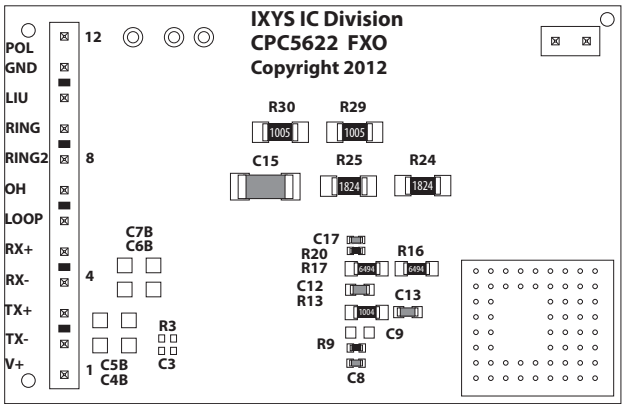


Figure 6. Bottom Side Components



The principal circuit components are listed below:

1. (U1) CPC5622A LITELINK
2. (Q1) CPC5603C FET
3. (U2) CPC5712U
4. (D1) Bridge Rectifier
5. (Q2) Circuit Protector
6. FET Heatsink - Top side: Bottom left corner; Bottom side: Bottom right corner.

5.2 CPC5622-EVAL-600R Parts List

Item	Qty.	Reference Designator	Value	Tolerance	Voltage	Power	Size
1	1	C1	10µF	10%	10V		1206
2	7	C2, C4a, C5a, C6a, C7a, C8, C18	100nF	10%	16V		0402
3	1	C3	DNP	10%	16V		0402
4	4	C4b, C5b, C6b, C7b	DNP	10%	16V		0805
5	1	C9	DNP	5%	16V		0603
6	1	C10	100pF	5%	50V		0402
7	1	C11	100nF	5%	50V		0603
8	2	C12, C13	10nF	5%	100V		0603
9	1	C14	10nF	10%	500V		0805
10	2	C15, C16	220pF	5%	2000V		1808
11	1	C17	15pF	5%	50V		0402
12	1	D1	S1ZB60		600V		S1ZB60
13	1	F1	DNP		250V		FUSE_461
14	1	J1	CON2_FXO				SIP-2P
15	1	J2	CON12_FXO				SIP-12P
16	1	Q1	CPC5603C		415V		SOT223
17	1	Q2	395V		395V		DO-214AA_S
18	2	R1, R21	2	5%		1/16W	0402
19	1	R2	191K	1%		1/16W	0402
20	2	R3, R4	DNP	1%		1/16W	0402
21	1	R5	137K	1%		1/16W	0402
22	1	R6	3.32K	1%		1/16W	0402
23	1	R7	49.9	1%		1/16W	0402
24	1	R8	301	1%		1/16W	0402
25	1	R9	0	1%		1/16W	0402
26	1	R10	143K	1%		1/16W	0402
27	1	R11	261K	1%		1/16W	0402
28	1	R12	499K	1%		1/16W	0402
29	1	R13	1M	1%		1/8W	0805
30	1	R14	1.82M	1%		1/16W	0402
31	1	R15	6.98	1%		1/8W	0805
32	2	R16, R17	6.49M	1%		1/8W	0805
33	1	R18	68.1	1%		1/16W	0402
34	1	R19	210K	1%		1/16W	0402
35	1	R20	232K	1%		1/16W	0402
36	4	R22, R23, R24, R25	1.82M	1%		1/4W	1206
37	1	R26	1.5M	1%		1/16W	0402
38	4	R27, R28, R29, R30	10M	1%		1/4W	1206
39	1	R31	806K	1%		1/16W	0402
40	2	R32, R35	26.7K	1%		1/16W	0402
41	1	R33	17.8K	1%		1/16W	0402
42	1	R34	80.6K	1%		1/16W	0402
43	1	R36	118K	1%		1/16W	0402
44	1	U1	CPC5622A				SOIC32
45	1	U2	CPC5712U				SOP16

NOTES: DNP (Do Not Populate) indicates the component is not installed on the board for this model.
Resistors with Tolerance = 1% have a Temperature Coefficient of +/- 100 PPM / °C; resistors with Tolerance = 5% have a Temperature Coefficient = 200 PPM / °C.
Capacitors with Value ≤ 1000pF are NPO / COG; all other capacitors are X7R.

6. LITELINK Design Resources

The schematic and printed circuit board design files can be found on the IXYS IC Division web site. They contain design specifications and notes to help guide you through your own design.

You will notice the values for many of the components have been altered from those shown in our other documentation. This is necessary to provide the noise cancellation feature not available in the application circuits presented in the legacy documentation. A formatted BOM used to assemble the evaluation boards can be found in the on-line design files.

To use the noise cancellation method presented in the CPC5622-EVAL-600R evaluation board it is necessary to follow the layout design fairly closely. The capacitive coupling of the NTS node to the low voltage side ground is a function of the PCB capacitor's copper shapes and separations. Additionally, parasitic capacitive coupling between NTS and the nets on the high voltage line side will reduce the desired coupling between NTS and the low voltage side ground. Changes to either the desired or parasitic capacitive coupling may require retuning of the cancellation circuit.

For additional information please visit www.ixysic.com

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