

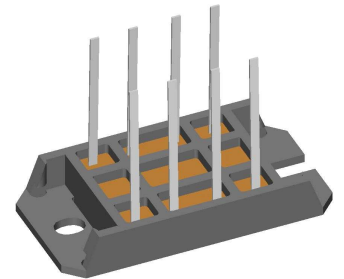
Thyristor Module

3~ Rectifier	
$V_{RRM} =$	1600 V
$I_{DAV} =$	45 A
$I_{FSM} =$	320 A

3~ Rectifier Bridge, half-controlled (high-side)

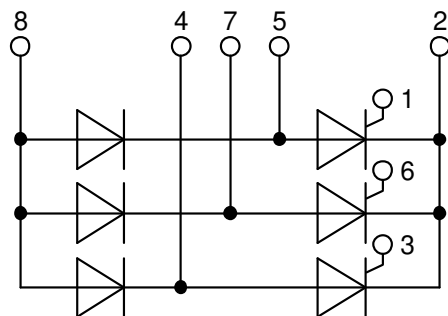
Part number

VVZ40-16io1



Backside: isolated

 E72873



Features / Advantages:

- Package with DCB ceramic base plate
- Improved temperature and power cycling
- Planar passivated chips
- Very low forward voltage drop
- Very low leakage current

Applications:

- Line rectifying 50/60 Hz
- Drives
- SMPS
- UPS

Package: V1-B-Pack

- Isolation Voltage: 3600 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Height: 10 mm
- Base plate: DCB ceramic
- Reduced weight
- Advanced power cycling

Disclaimer Notice

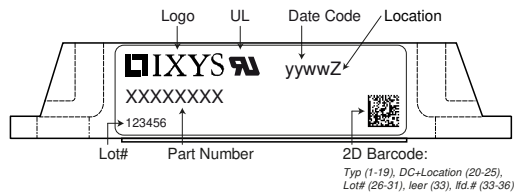
Information furnished is believed to be accurate and reliable. However, users should independently evaluate the suitability of and test each product selected for their own applications. Littelfuse products are not designed for, and may not be used in, all applications. Read complete Disclaimer Notice at www.littelfuse.com/disclaimer-electronics.



Rectifier			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1700	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1600	V
I_{RD}	reverse current, drain current	$V_{R/D} = 1600 V$	$T_{VJ} = 25^{\circ}C$		300	μA
		$V_{R/D} = 1600 V$	$T_{VJ} = 125^{\circ}C$		5	mA
V_T	forward voltage drop	$I_T = 15 A$	$T_{VJ} = 25^{\circ}C$		1.12	V
		$I_T = 45 A$			1.47	V
		$I_T = 15 A$	$T_{VJ} = 125^{\circ}C$		1.07	V
		$I_T = 45 A$			1.52	V
I_{DAV}	bridge output current	$T_C = 100^{\circ}C$ rectangular $d = 1/3$	$T_{VJ} = 125^{\circ}C$		45	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 125^{\circ}C$		0.85	V
r_T	slope resistance				15	m Ω
R_{thJC}	thermal resistance junction to case				1	K/W
R_{thCH}	thermal resistance case to heatsink			0.6		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}C$		100	W
I_{TSM}	max. forward surge current	$t = 10 ms$; (50 Hz), sine	$T_{VJ} = 45^{\circ}C$		320	A
		$t = 8,3 ms$; (60 Hz), sine	$V_R = 0 V$		345	A
		$t = 10 ms$; (50 Hz), sine	$T_{VJ} = 125^{\circ}C$		270	A
		$t = 8,3 ms$; (60 Hz), sine	$V_R = 0 V$		295	A
I^2t	value for fusing	$t = 10 ms$; (50 Hz), sine	$T_{VJ} = 45^{\circ}C$		510	A ² s
		$t = 8,3 ms$; (60 Hz), sine	$V_R = 0 V$		495	A ² s
		$t = 10 ms$; (50 Hz), sine	$T_{VJ} = 125^{\circ}C$		365	A ² s
		$t = 8,3 ms$; (60 Hz), sine	$V_R = 0 V$		360	A ² s
C_J	junction capacitance	$V_R = 400 V$ $f = 1 MHz$	$T_{VJ} = 25^{\circ}C$		16	pF
P_{GM}	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 125^{\circ}C$		10	W
		$t_p = 300 \mu s$			1	W
P_{GAV}	average gate power dissipation				0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 125^{\circ}C$; $f = 50 Hz$ repetitive, $I_T = 45 A$			150	A/ μs
		$t_p = 200 \mu s$; $di_G/dt = 0.3 A/\mu s$; $I_G = 0.3 A$; $V = 2/3 V_{DRM}$ non-repet., $I_T = 15 A$			500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = 2/3 V_{DRM}$ $R_{GK} = \infty$; method 1 (linear voltage rise)	$T_{VJ} = 125^{\circ}C$		1000	V/ μs
V_{GT}	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1	V
			$T_{VJ} = -40^{\circ}C$		1.2	V
I_{GT}	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		65	mA
			$T_{VJ} = -40^{\circ}C$		80	mA
V_{GD}	gate non-trigger voltage	$V_D = 2/3 V_{DRM}$	$T_{VJ} = 125^{\circ}C$		0.2	V
I_{GD}	gate non-trigger current				5	mA
I_L	latching current	$t_p = 30 \mu s$	$T_{VJ} = 25^{\circ}C$		150	mA
		$I_G = 0.3 A$; $di_G/dt = 0.3 A/\mu s$				
I_H	holding current	$V_D = 6 V$ $R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		100	mA
t_{gd}	gate controlled delay time	$V_D = 1/2 V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	μs
		$I_G = 0.3 A$; $di_G/dt = 0.3 A/\mu s$				
t_q	turn-off time	$V_R = 100 V$; $I_T = 15 A$; $V = 2/3 V_{DRM}$ $di/dt = 10 A/\mu s$ $dv/dt = 20 V/\mu s$ $t_p = 300 \mu s$	$T_{VJ} = 100^{\circ}C$		150	μs



Package V1-B-Pack		Ratings				
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal			100	A
T_{VJ}	virtual junction temperature		-40		125	°C
T_{op}	operation temperature		-40		100	°C
T_{stg}	storage temperature		-40		125	°C
Weight				30		g
M_D	mounting torque		2		2.5	Nm
$d_{Spp/App}$	creepage distance on surface / striking distance through air	terminal to terminal	6.0			mm
$d_{Spb/Apb}$		terminal to backside	12.0			mm
V_{ISOL}	isolation voltage	t = 1 second	3600			V
		t = 1 minute	3000			V



Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	VVZ40-16io1	VVZ40-16io1	Box	5	466379

Equivalent Circuits for Simulation

* on die level

$T_{VJ} = 125^{\circ}C$

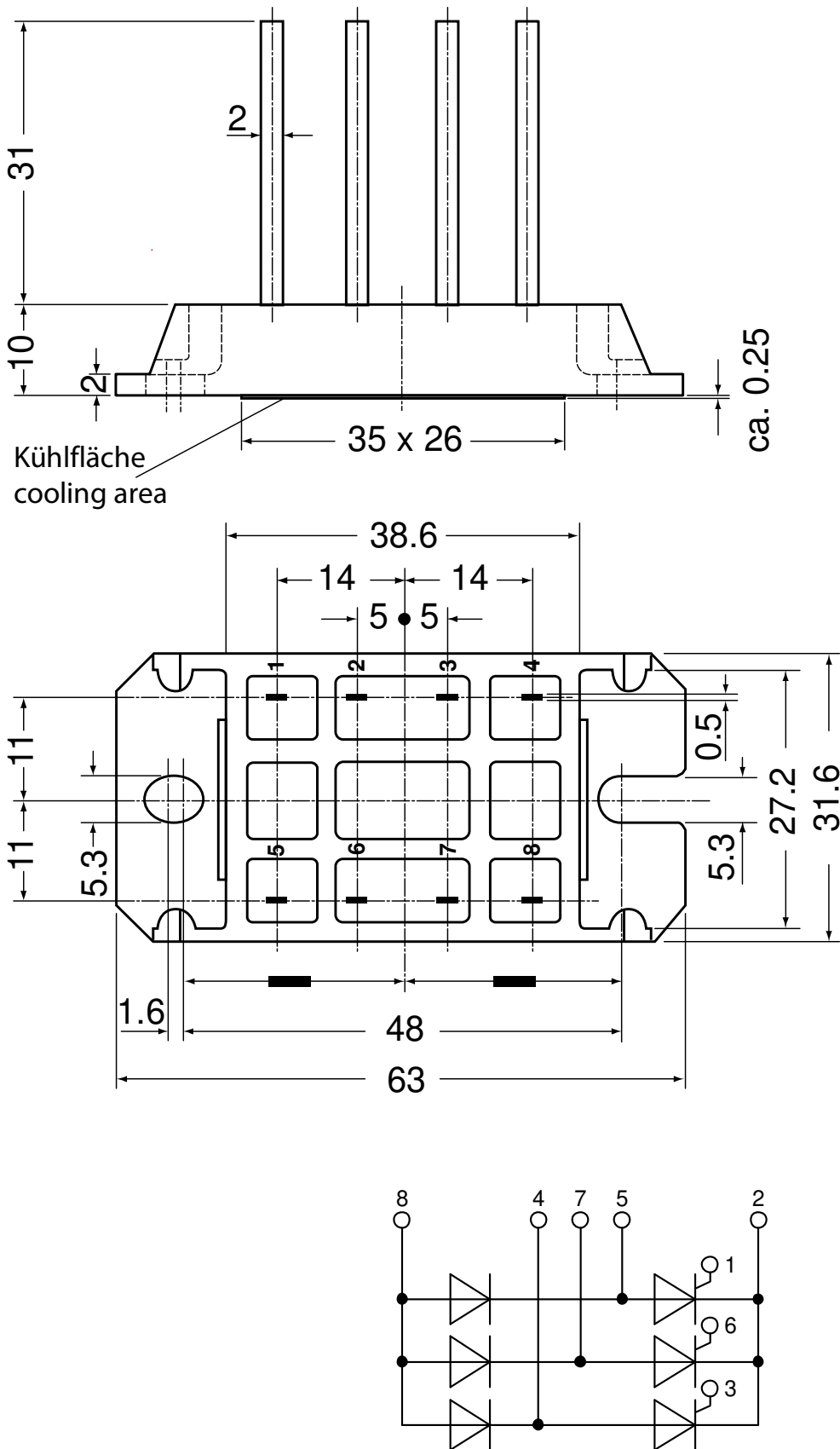


Thyristor

$V_{0\ max}$	threshold voltage	0.85	V
$R_{0\ max}$	slope resistance *	12.5	mΩ



Outlines V1-B-Pack



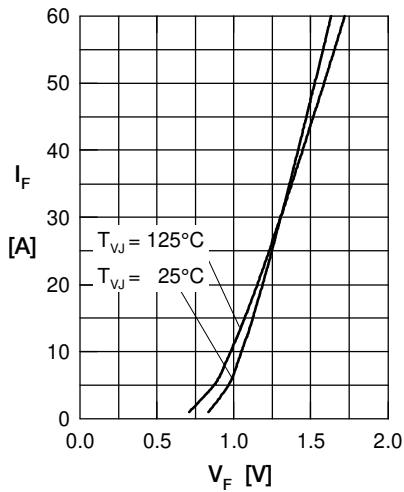
Thyristor


Fig. 1 Forward current vs. voltage drop per thyristor

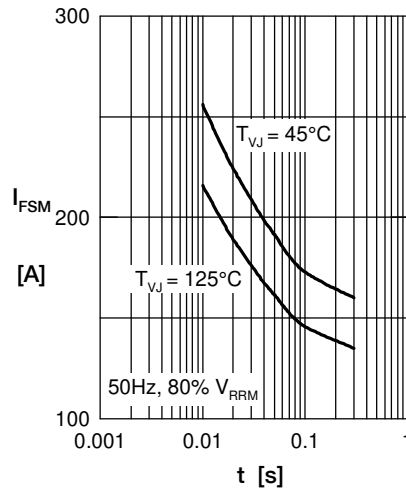


Fig. 2 Surge overload current vs. time per thyristor

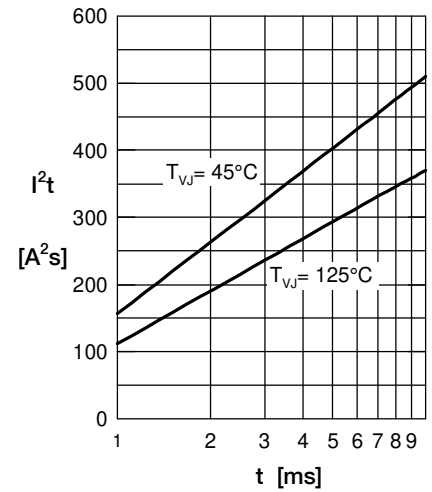
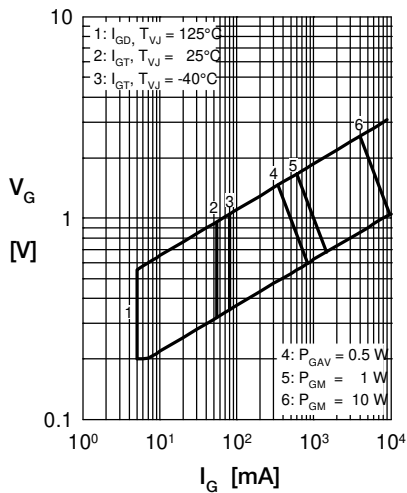

 Fig. 3 I^2t vs. time per thyristor


Fig. 4 Gate trigger characteristics

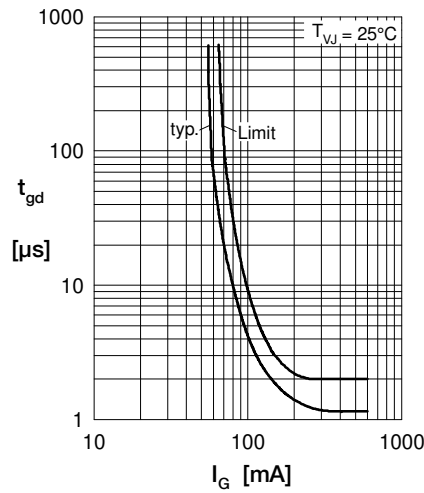


Fig. 5 Gate trigger delay time

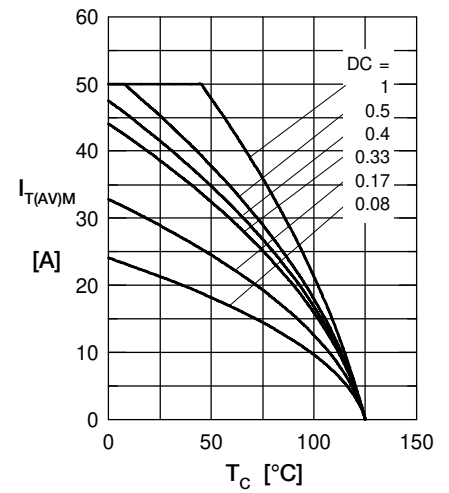


Fig. 5 Max. forward current vs. case temperature per thyristor

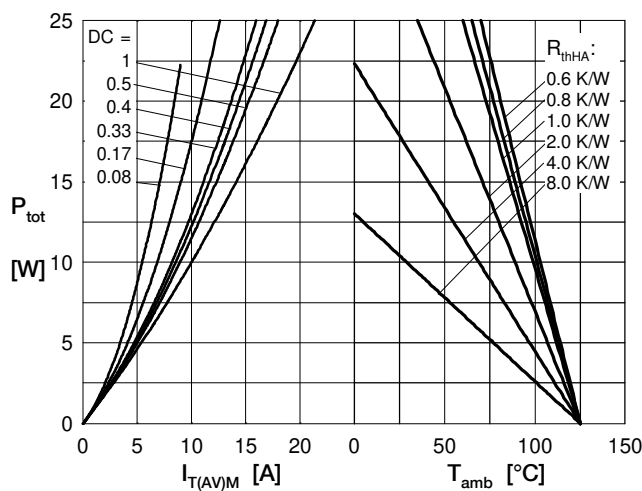


Fig. 4 Power dissipation vs. forward current and ambient temperature per thyristor

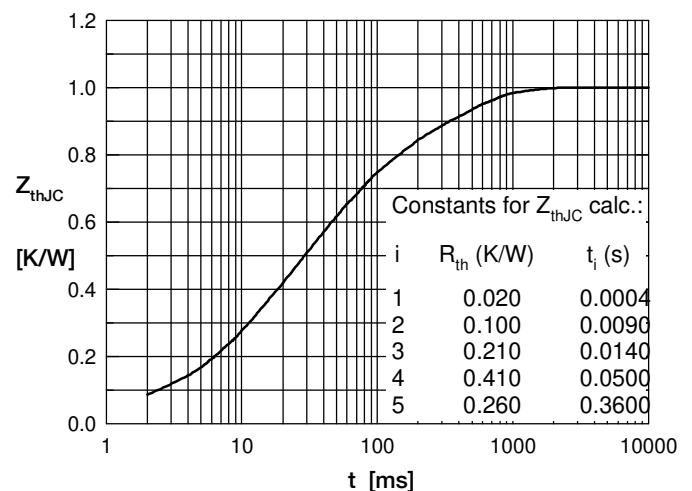


Fig. 6 Transient thermal impedance junction to case vs. time per thyristor