High Efficiency Thyristor

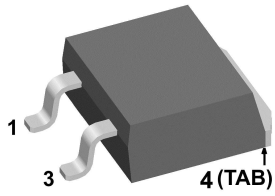
V_{RRM}	=	1200 V
I_{TAV}	=	40 A
V_T	=	1.26 V

Single Anode Gated Thyristor

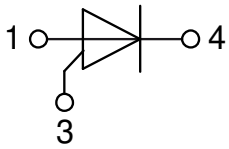
Part number

CLB40I1200PZ

Marking on Product: CLB40I1200PZ



Backside: cathode



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Thyristor can be used as Triac
  - anti-parallel combination with CGT
  - Cathode-Gated-Thyristor covers quadrants I & II
  - CGT-counterpart: CLA40E1200NPZ

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: TO-263 (D2Pak-HV)

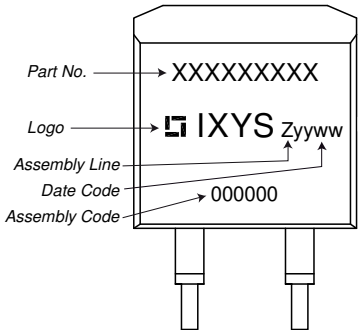
- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

Thyristor

Symbol	Definition	Conditions		Ratings min.	typ.	max.	Unit
$V_{RSM/DSM}$	*max. non-repetitive reverse/forward blocking voltage*		T_{VJ} = 25°C			1300	V
$V_{RRM/DRM}$	*max. repetitive reverse/forward blocking voltage*		T_{VJ} = 25°C			1200	V
$I_{R/D}$	*reverse current, drain current*	$V_{R/D}$ = 1200 V	T_{VJ} = 25°C			10	µA
		$V_{R/D}$ = 1200 V	T_{VJ} = 125°C			2	mA
V_T	*forward voltage drop*	I_T = 40 A	T_{VJ} = 25°C			1.30	V
		I_T = 80 A				1.59	V
		I_T = 40 A	T_{VJ} = 125°C			1.26	V
		I_T = 80 A				1.64	V
I_{TAV}	*average forward current*	T_C = 125°C	T_{VJ} = 150°C			40	A
$I_{T(RMS)}$	*RMS forward current*	180° sine				63	A
V_{T0}	*threshold voltage* } *for power loss calculation only*		T_{VJ} = 150°C			0.85	V
r_T	*slope resistance* }					9.9	mΩ
R_{thJC}	*thermal resistance junction to case*					0.4	K/W
R_{thCH}	*thermal resistance case to heatsink*				0.25		K/W
P_{tot}	*total power dissipation*		T_C = 25°C			310	W
I_{TSM}	*max. forward surge current*	t = 10 ms; (50 Hz), sine	T_{VJ} = 45°C			520	A
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			560	A
		t = 10 ms; (50 Hz), sine	T_{VJ} = 150°C			440	A
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			475	A
I^2t	*value for fusing*	t = 10 ms; (50 Hz), sine	T_{VJ} = 45°C			1.35	kA²s
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			1.31	kA²s
		t = 10 ms; (50 Hz), sine	T_{VJ} = 150°C			970	A²s
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			940	A²s
C_J	*junction capacitance*	V_R = 400 V f = 1 MHz	T_{VJ} = 25°C		22		pF
P_{GM}	*max. gate power dissipation*	t_P = 30 µs	T_C = 150°C			10	W
		t_P = 300 µs				5	W
P_{GAV}	*average gate power dissipation*					0.5	W
$(di/dt)_{cr}$	*critical rate of rise of current*	T_{VJ} = 150°C; f = 50 Hz	repetitive, I_T = 120 A			150	A/µs
		t_P = 200 µs; di_G/dt = 0.3 A/µs;					
		I_G = 0.3 A; V = ⅔ V_{DRM}	non-repet., I_T = 40 A			500	A/µs
$(dv/dt)_{cr}$	*critical rate of rise of voltage*	V = ⅔ V_{DRM}	T_{VJ} = 150°C			500	V/µs
		R_{GK} = ∞; method 1 (linear voltage rise)					
V_{GT}	*gate trigger voltage*	V_D = 6 V	T_{VJ} = 25°C			1.7	V
			T_{VJ} = -40°C			1.9	V
I_{GT}	*gate trigger current*	V_D = 6 V	T_{VJ} = 25°C			30	mA
			T_{VJ} = -40°C			50	mA
V_{GD}	*gate non-trigger voltage*	V_D = ⅔ V_{DRM}	T_{VJ} = 150°C			0.2	V
I_{GD}	*gate non-trigger current*					1	mA
I_L	*latching current*	t_p = 10 µs	T_{VJ} = 25°C			100	mA
		I_G = 0.3 A; di_G/dt = 0.3 A/µs					
I_H	*holding current*	V_D = 6 V R_{GK} = ∞	T_{VJ} = 25°C			70	mA
t_{gd}	*gate controlled delay time*	V_D = ½ V_{DRM}	T_{VJ} = 25°C			2	µs
		I_G = 0.3 A; di_G/dt = 0.3 A/µs					
t_q	*turn-off time*	V_R = 100 V; I_T = 40 A; V = ⅔ V_{DRM}	T_{VJ} = 125 °C		150		µs
		di/dt = 10 A/µs dv/dt = 20 V/µs t_p = 200 µs					

Package TO-263 (D2Pak-HV)			Ratings			
Symbol	**Definition**	**Conditions**	**min.**	**typ.**	**max.**	**Unit**
I_{RMS}	*RMS current*	per terminal			35	A
T_{VJ}	*virtual junction temperature*		-40		150	°C
T_{op}	*operation temperature*		-40		125	°C
T_{stg}	*storage temperature*		-40		150	°C
Weight				1.5		g
F_C	*mounting force with clip*		20		60	N
$d_{Spp/App}$	*creepage distance on surface | striking distance through air*	*terminal to terminal*	4.2			mm
$d_{Spb/Apb}$		*terminal to backside*	4.7			mm

Product Marking



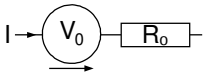
Part description

C = Thyristor (SCR)
L = High Efficiency Thyristor
B = Anode gated (up to 1200V)
40 = Current Rating [A]
I = Single Anode Gated Thyristor
1200 = Reverse Voltage [V]
PZ = TO-263AB (D2Pak) (2HV)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLB40I1200PZ-TRL	CLB40I1200PZ	Tape & Reel	800	518476
Alternative	CLB40I1200PZ-TUB	CLB40I1200PZ	Tube	50	525290

Equivalent Circuits for Simulation

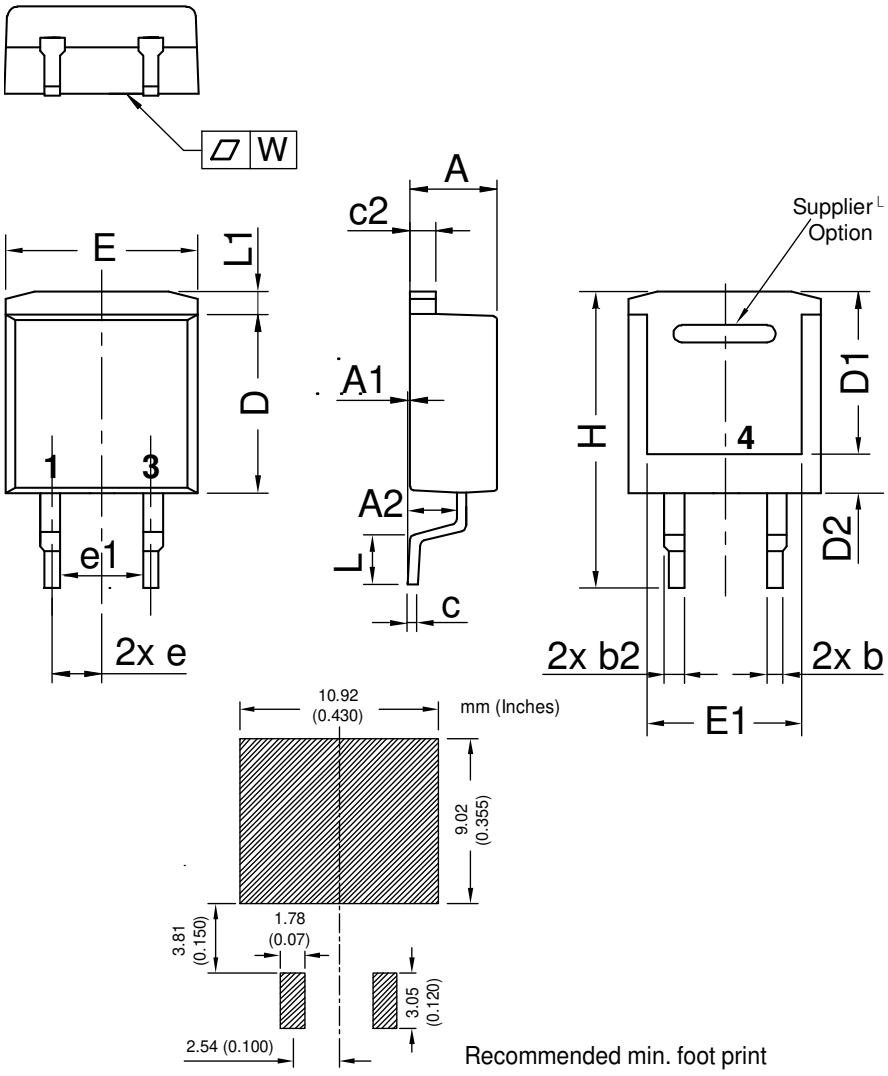
** on die level* T_{VJ} = 150 °C



Thyristor

$V_{0\,max}$	*threshold voltage*	0.85	V
$R_{0\,max}$	*slope resistance **	7.4	mΩ

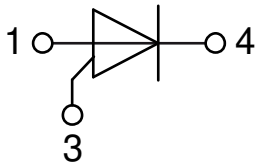
Outlines TO-263 (D2Pak-HV)



Recommended min. foot print

Dim.	Millimeter		Inches	
	min	max	min	max
A	4.06	4.83	0.160	0.190
A1	typ. 0.10		typ. 0.004	
A2	2.41		0.095	
b	0.51	0.99	0.020	0.039
b2	1.14	1.40	0.045	0.055
c	0.40	0.74	0.016	0.029
c2	1.14	1.40	0.045	0.055
D	8.38	9.40	0.330	0.370
D1	8.00	8.89	0.315	0.350
D2	2.3		0.091	
E	9.65	10.41	0.380	0.410
E1	6.22	8.50	0.245	0.335
e	2,54 BSC		0,100 BSC	
e1	4.28		0.169	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	1.02	1.68	0.040	0.066
W	typ. 0.02	0.040	typ. 0.0008	0.002

All dimensions conform with and/or within JEDEC standard.



Thyristor

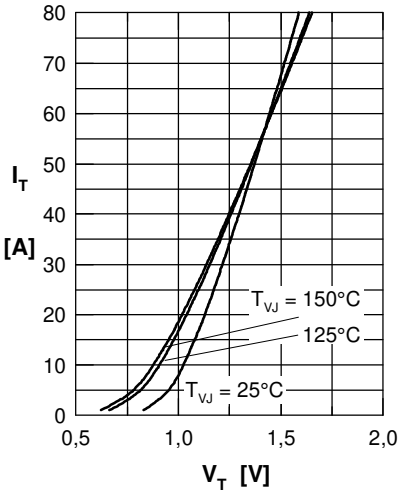


Fig. 1 Forward characteristics

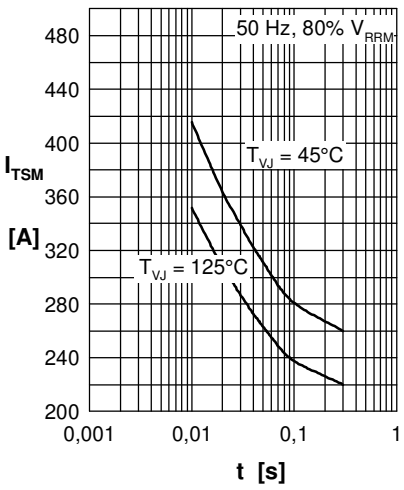


Fig. 2 Surge overload current
I_{TSM}: crest value, t: duration

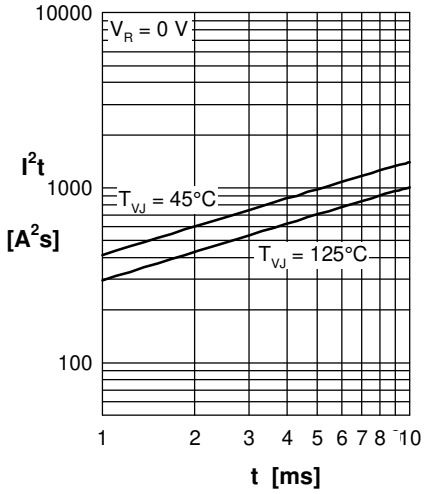


Fig. 3 I^2t versus time (1-10 s)

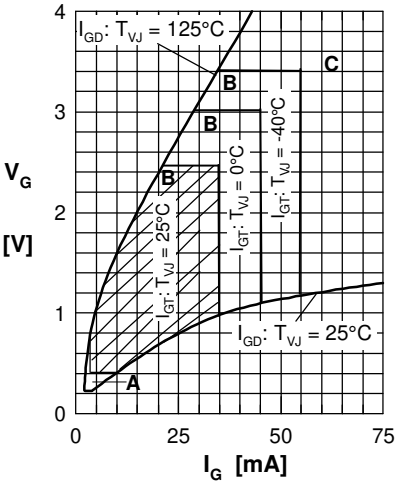


Fig. 4 Gate voltage & gate current
Triggering: A = no; B = possible; C = safe

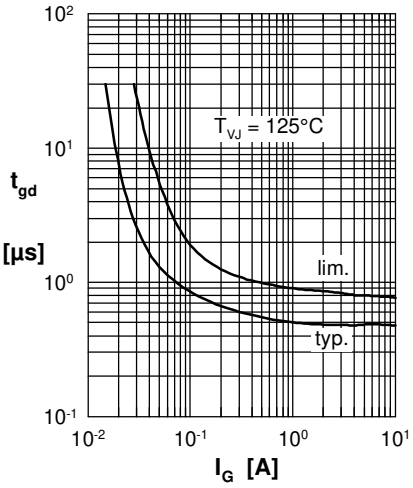


Fig. 5 Gate controlled delay time t_{gd}

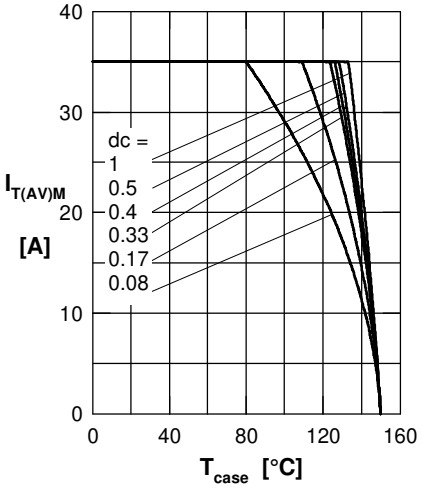


Fig. 6 Max. forward current at case temperature

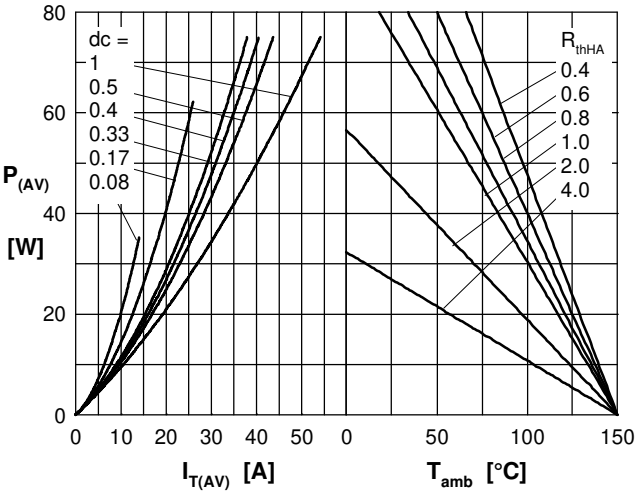
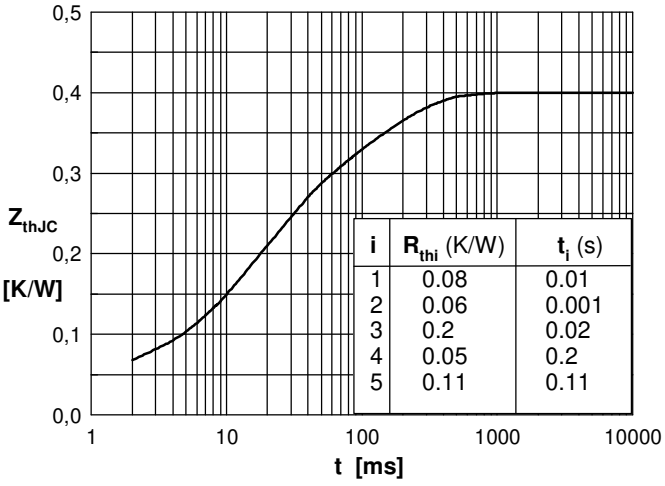


Fig. 7a Power dissipation versus direct output current
Fig. 7b and ambient temperature



i	R_{thi} (K/W)	t_i (s)
1	0.08	0.01
2	0.06	0.001
3	0.2	0.02
4	0.05	0.2
5	0.11	0.11

Fig. 7 Transient thermal impedance junction to case