

High Efficiency Thyristor

$$V_{RRM} = 1200 \text{ V}$$

$$I_{TAV} = 40 \text{ A}$$

$$V_T = 1.23 \text{ V}$$

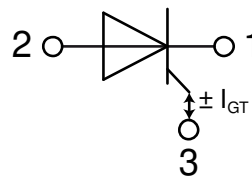
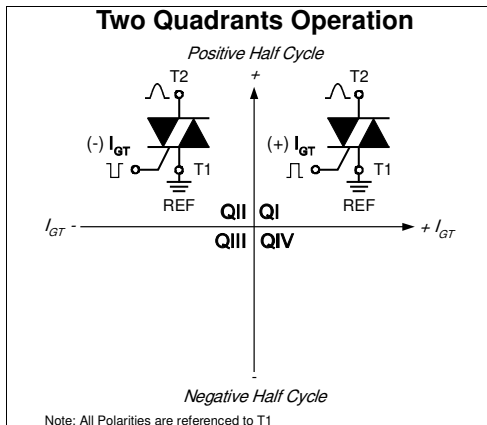
Two Quadrants Operation QI & QII
 Single Thyristor with two gate polarities

Part number

CLA40E1200NHB



Backside: anode



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Two gate current polarities usable
 - positive -> quadrant I
 - negative -> quadrant II
- Thyristor can be used as Triac
 - anti-parallel combination with AGT
 - Anode-Gated-Thyristor covers quadrant III
 - AGT-counterpart: CLB40I1200PZ

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: TO-247

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

Disclaimer Notice

Information furnished is believed to be accurate and reliable. However, users should independently evaluate the suitability of and test each product selected for their own applications. Littelfuse products are not designed for, and may not be used in, all applications. Read complete Disclaimer Notice at www.littelfuse.com/disclaimer-electronics.

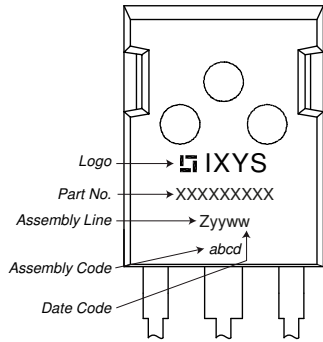


Thyristor			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1200	V
I_{RD}	reverse current, drain current	$V_{R/D} = 1200 V$	$T_{VJ} = 25^{\circ}C$		10	μA
		$V_{R/D} = 1200 V$	$T_{VJ} = 125^{\circ}C$		2	mA
V_T	forward voltage drop	$I_T = 40 A$	$T_{VJ} = 25^{\circ}C$		1.28	V
		$I_T = 80 A$			1.55	V
		$I_T = 40 A$	$T_{VJ} = 125^{\circ}C$		1.23	V
		$I_T = 80 A$			1.59	V
I_{TAV}	average forward current	$T_C = 120^{\circ}C$	$T_{VJ} = 150^{\circ}C$		40	A
$I_{T(RMS)}$	RMS forward current	180° sine			63	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}C$		0.85	V
r_T	slope resistance				9.2	m Ω
R_{thJC}	thermal resistance junction to case				0.4	K/W
R_{thCH}	thermal resistance case to heatsink			0.25		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}C$		310	W
I_{TSM}	max. forward surge current	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		520	A
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		560	A
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		440	A
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		475	A
I^2t	value for fusing	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		1.35	kA ² s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		1.31	kA ² s
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		970	A ² s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		940	A ² s
C_J	junction capacitance	$V_R = 400 V \quad f = 1 \text{ MHz}$	$T_{VJ} = 25^{\circ}C$		19	pF
P_{GM}	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 150^{\circ}C$		10	W
		$t_p = 300 \mu s$			5	W
P_{GAV}	average gate power dissipation				0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 150^{\circ}C; f = 50 \text{ Hz}$	repetitive, $I_T = 120 A$		150	A/ μs
		$t_p = 200 \mu s; di_G/dt = 0.3 A/\mu s;$ $I_G = 0.3 A; V = \frac{2}{3} V_{DRM}$	non-repet., $I_T = 40 A$		500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}C$		500	V/ μs
		$R_{GK} = \infty; \text{method 1 (linear voltage rise)}$				
V_{GT}	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1.7	V
			$T_{VJ} = -40^{\circ}C$		1.9	V
I_{GT}	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		± 35	mA
			$T_{VJ} = -40^{\circ}C$		± 55	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}C$		0.2	V
I_{GD}	gate non-trigger current				± 1	mA
I_L	latching current	$t_p = 10 \mu s$	$T_{VJ} = 25^{\circ}C$		100	mA
		$I_G = 0.3 A; di_G/dt = 0.3 A/\mu s$				
I_H	holding current	$V_D = 6 V \quad R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		70	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	μs
		$I_G = 0.3 A; di_G/dt = 0.3 A/\mu s$				
t_q	turn-off time	$V_R = 100 V; I_T = 40 A; V = \frac{2}{3} V_{DRM}$ $di/dt = 10 A/\mu s \quad dv/dt = 20 V/\mu s \quad t_p = 200 \mu s$	$T_{VJ} = 125^{\circ}C$		150	μs



Package TO-247			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal			70	A
T_{VJ}	virtual junction temperature		-40		150	°C
T_{op}	operation temperature		-40		125	°C
T_{stg}	storage temperature		-40		150	°C
Weight				6		g
M_D	mounting torque		0.8		1.2	Nm
F_C	mounting force with clip		20		120	N

Product Marking



Part description

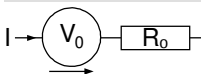
- C = Thyristor (SCR)
- L = High Efficiency Thyristor
- A = (up to 1200V)
- 40 = Current Rating [A]
- E = Single Thyristor with two gate polarities
- 1200 = Reverse Voltage [V]
- N = Three Quadrants operation: QI - QIII
- HB = TO-247AD (3)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA40E1200NHB	CLA40E1200NHB	Tube	30	524548

Equivalent Circuits for Simulation

* on die level

$T_{VJ} = 150\text{ °C}$



Thyristor

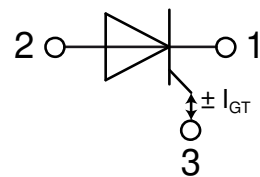
$V_{0\ max}$	threshold voltage	0.85	V
$R_{0\ max}$	slope resistance *	6.7	mΩ



Outlines TO-247



Sym.	Inches		Millimeter	
	min.	max.	min.	max.
A	0.185	0.209	4.70	5.30
A1	0.087	0.102	2.21	2.59
A2	0.059	0.098	1.50	2.49
D	0.819	0.845	20.79	21.45
E	0.610	0.640	15.48	16.24
E2	0.170	0.216	4.31	5.48
e	0.215 BSC		5.46 BSC	
L	0.780	0.800	19.80	20.30
L1	-	0.177	-	4.49
Ø P	0.140	0.144	3.55	3.65
Q	0.212		5.38	
S	0.242 BSC		6.14 BSC	
b	0.039	0.055	0.99	1.40
b2	0.065	0.094	1.65	2.39
b4	0.102	0.135	2.59	3.43
c	0.015	0.035	0.38	0.89
D1	0.515	-	13.07	-
D2	0.020	0.053	0.51	1.35
E1	0.530	-	13.45	-
Ø P1	-	0.29	-	7.39



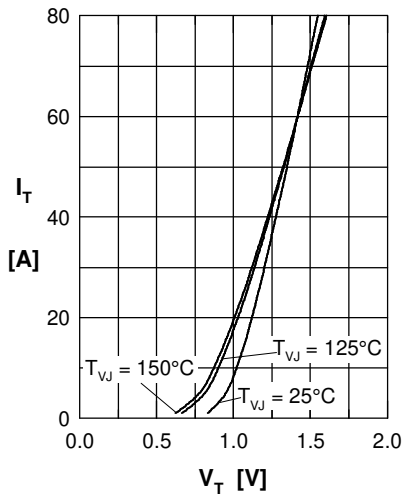
Thyristor


Fig. 1 Forward characteristics

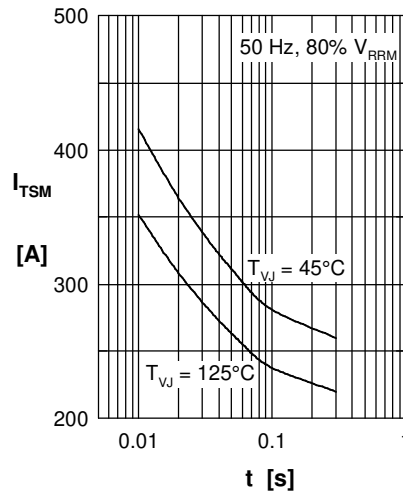
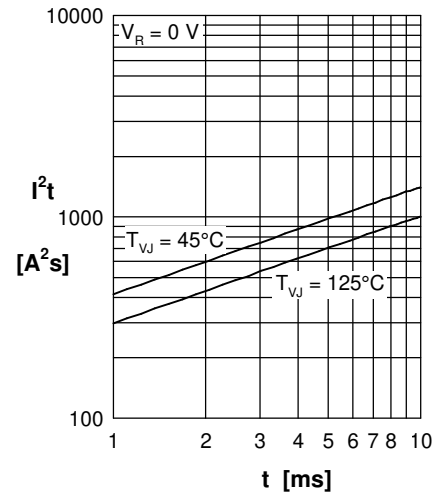
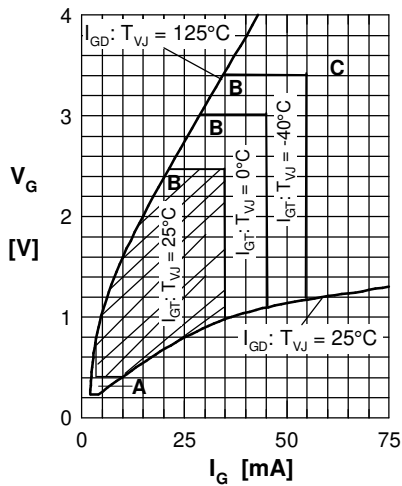

 Fig. 2 Surge overload current
 I_{TSM} : crest value, t : duration

 Fig. 3 I^2t versus time (1-10 s)


Fig. 4 Gate voltage & gate current

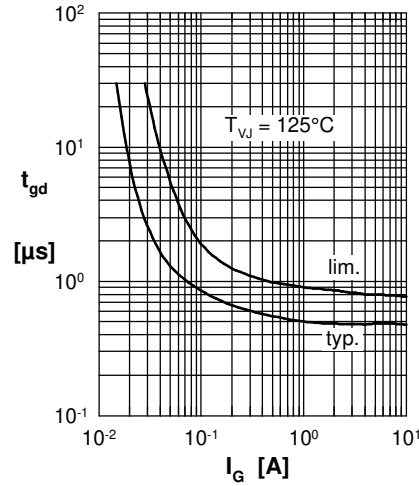
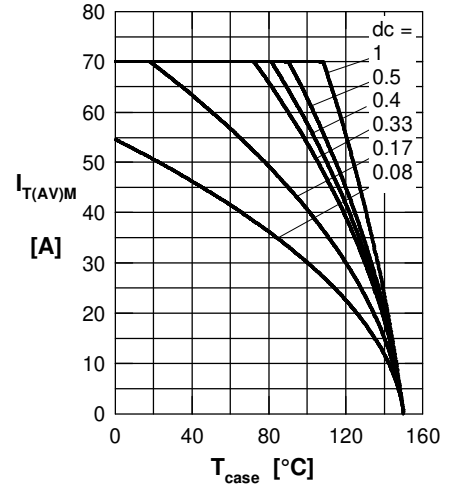

 Fig. 5 Gate controlled delay time t_{gd}


Fig. 6 Max. forward current at case temperature

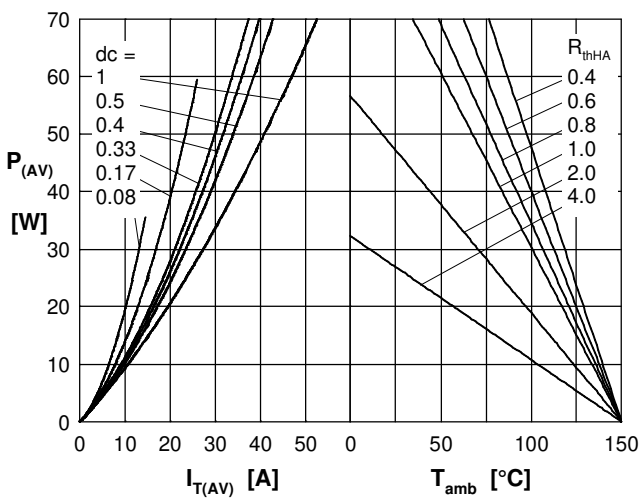
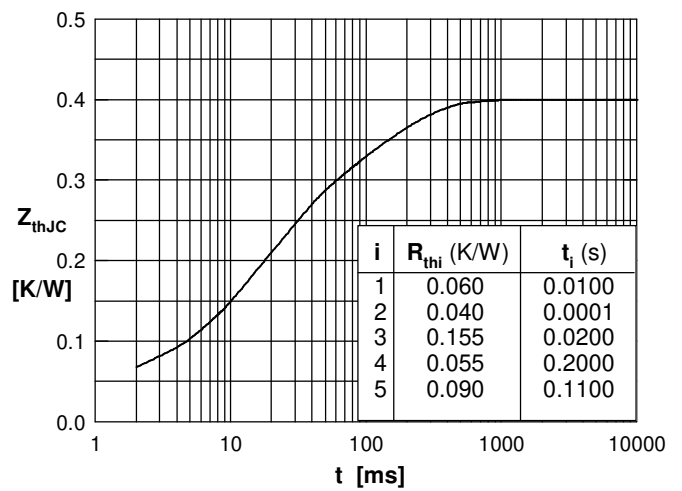

 Fig. 7a Power dissipation versus direct output current
 Fig. 7b and ambient temperature


Fig. 7 Transient thermal impedance junction to case

