ISOPLUS – SMPD: An Advanced Isolated Packaging to Fully Exploit the Advantages of SiC MOSFETs

Abstract

Power semiconductors are typically delivered in two types of packages – discrete and module. Each type is limited by its own anatomical and functional capabilities. Discrete devices tend to be highly standardized, are suitable for automated production, and mostly limited to single switch configurations. Power modules can incorporate complete topologies but require more complex handling. To bridge the gap between the two, Littelfuse offers an advanced isolated package, the Surface Mount Power Device (SMPD), delivering the performance of a power module with the design and mounting flexibility of a discrete. SMPDs are available embedding standard power electronics building blocks to realize full topologies by distributed arrangement of functional groups. This document compares the dynamic performance of the SMPD versus standard discrete packaging. It especially highlights the advantages of the SMPD in combination with Silicon Carbide (SiC) MOSFET. Thermal measurements comparing SMPDs with different ceramics with a standard TO-247 package show that SMPDs are the ideal choice to minimize chip junction temperatures and junction-heatsink thermal resistances. The better thermal performance of the SMPD supports an increase of the power output in applications for a given chip rating and unlocks system-level cost savings.

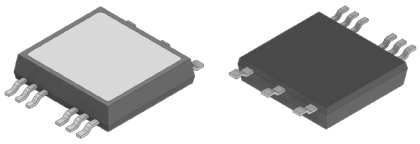

Figure 1.Surface Mount Power Device (SMPD)

Applications

- Industrial switch mode power supplies
- Industrial motor drives
- High-frequency applications: induction heating, plasma and process power supplies
- EVs and EV charging infrastructure
- Solar inverters
- HVAC and heat pumps
- Battery and energy storage systems, uninterruptible power supply

Target Audience

This document is intended for power electronics engineers and design enthusiasts.

Contact Information

For more information on this topic, contact the Littelfuse Power Semiconductor team of product and applications experts:

- PowerSemiSupport@Littelfuse.com

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1. Introduction

With its advanced top side cooling, the Surface Mount Power Device (SMPD) was pioneered by Littelfuse in 2012. The SMPD as displayed in **Figure 2**, offers several key features and advantages:

- Integrated Direct Copper Bonded (DCB) isolation provides high reliability under power and temperature cycling environments [1]
- Isolation voltage rating of minimum 2.5 kV AC, 1 minute
- Optimized use of DCB area inside the component increases the power density and simplifies the thermal management
- Allows fully automated pick and place and standard reflow soldering for ease of manufacturing
- Reduced EMI attributed to the small chip-to-heatsink stray capacitance

The primary motivation to use SiC MOSFETs in an application is an increased power density, improved efficiency, and high frequency operation, leading to a compact and energy efficient design. To offset the higher costs of the SiC components, it is economically desirable to obtain the highest performance out of the chip. In this regard, standard discrete packages present limitations often related to thermal management.

Hence, the SMPD comes into play – a revolutionary package simplifying the way design engineers address their power semiconductor system integration and assembly needs. The SMPD is crafted to support a wide array of topologies, including, but not limited to, buck, boost, phase-leg, and other customized combinations. SMPDs are available in a variety of technologies such as Si/SiC MOSFET, IGBT, Diode, Thyristor, or TRIAC, in different voltage classes ranging from 40 V to 3000 V.

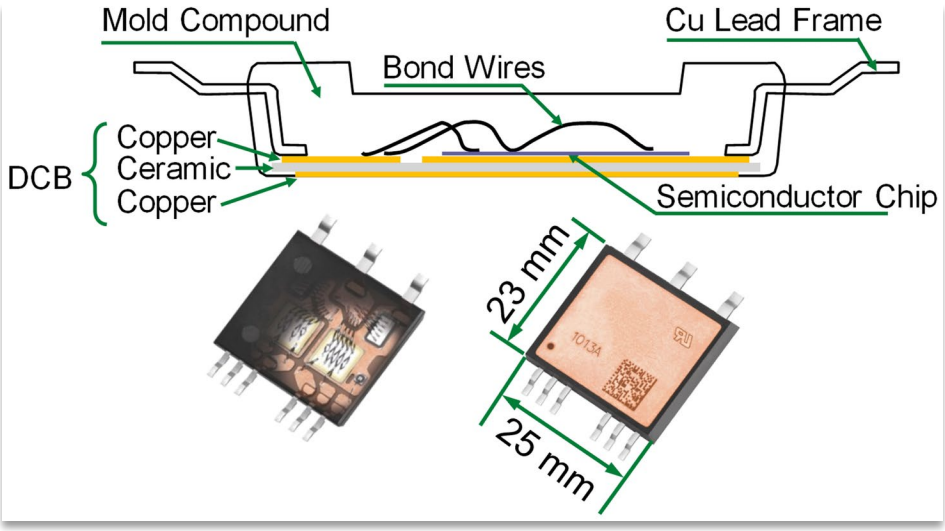

Figure 2. ISOPLUS – SMPD internal construction

2. Performance Advantages of SiC-based SMPD Compared to Standard Discretes

In comparing the dynamic behavior of a SiC MOSFET half bridge in SMPD with half bridges realized using standard discrete packages, the advantages offered by the former can easily be quantified. The measurements conducted in this experiment are based on a standard double pulse test setup as depicted in **Figure 3** and the dynamic characterization platform from Littelfuse [2]. The switching performance of the MOSFETs under test have been compared by measuring switching parameters such as switching time (t_{SW}) and switching energy (E_{SW}), as well as comparing the body-diode switching performance (recovery time, t_{rr}, maximum reverse current, I_{rm}, and reverse recovery energy, E_{rr}.)

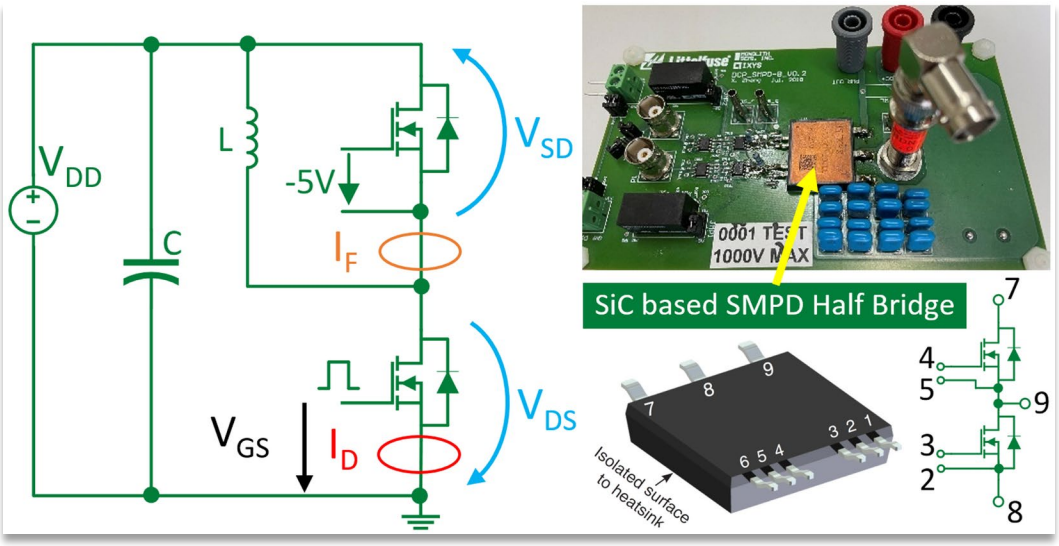

Figure 3. SMPD Dynamic Characterization Platform

The experimental setup was based on comparing 1200 V SiC MOSFETs in SMPD to MOSFETs in TO-247-3L, TO-263-7L, and TO-247-4L, as summarized in **Table 1**. All the devices are from comparable MOSFET chip technology generation, as visible from the on-state resistance, $R_{DS(on)}$, and the gate-source operating voltage $V_{GS,OP}$. It is important to note the actual differences in MOSFET dices used for the comparison – the SMPD and TO-247-3L share the same chip, while the TO-263-7L and TO-247-4L are devices from 3rd party manufacturers.

Table 1. Comparison of devices featuring SiC MOSFETs

	SMPD	TO-247 (3 Lead)	TO-263 (7 Lead)	TO-247 (4 Lead)
Configuration	Phase Leg	Single	Single	Single
SiC Die	Die A	Die A	Die B	Die C
$V_{(BR)DSS}$ (V)	1200	1200	1200	1200
$R_{DS(on)}$ (mΩ)	80	80	80	80
I_{D25} (A)	26	39	30	36
$V_{GS,OP}$ (V)	–5/+20	–5/+20	–5/+20	–5/+20

The measured waveforms of gate-source voltage, drain current, and body diode reverse recovery current are given in **Figure 4**. The gate voltage comparison reveals that the SMPD with kelvin source connection not only speeds up the charging of the gate capacitance, but due to its low package inductance, it eliminates gate oscillations at any given operating condition. The drain current comparison during turn-on reveals that the TO-247-4L and TO-263-7L devices have approximately a 25% higher peak current than the SMPD, despite having similar channel resistance $R_{DS(on)}$ and similar technology of MOSFET dice. From the body diode's reverse current comparison, it can be observed that even though they embed the same MOSFET chip, the SMPD achieves shorter reverse recovery time than the TO247-3L mainly due to the kelvin source connection. Due to this, the SMPD exhibits a smaller area under the body-diode recovery current curve, corresponding to lower losses in the body diode.

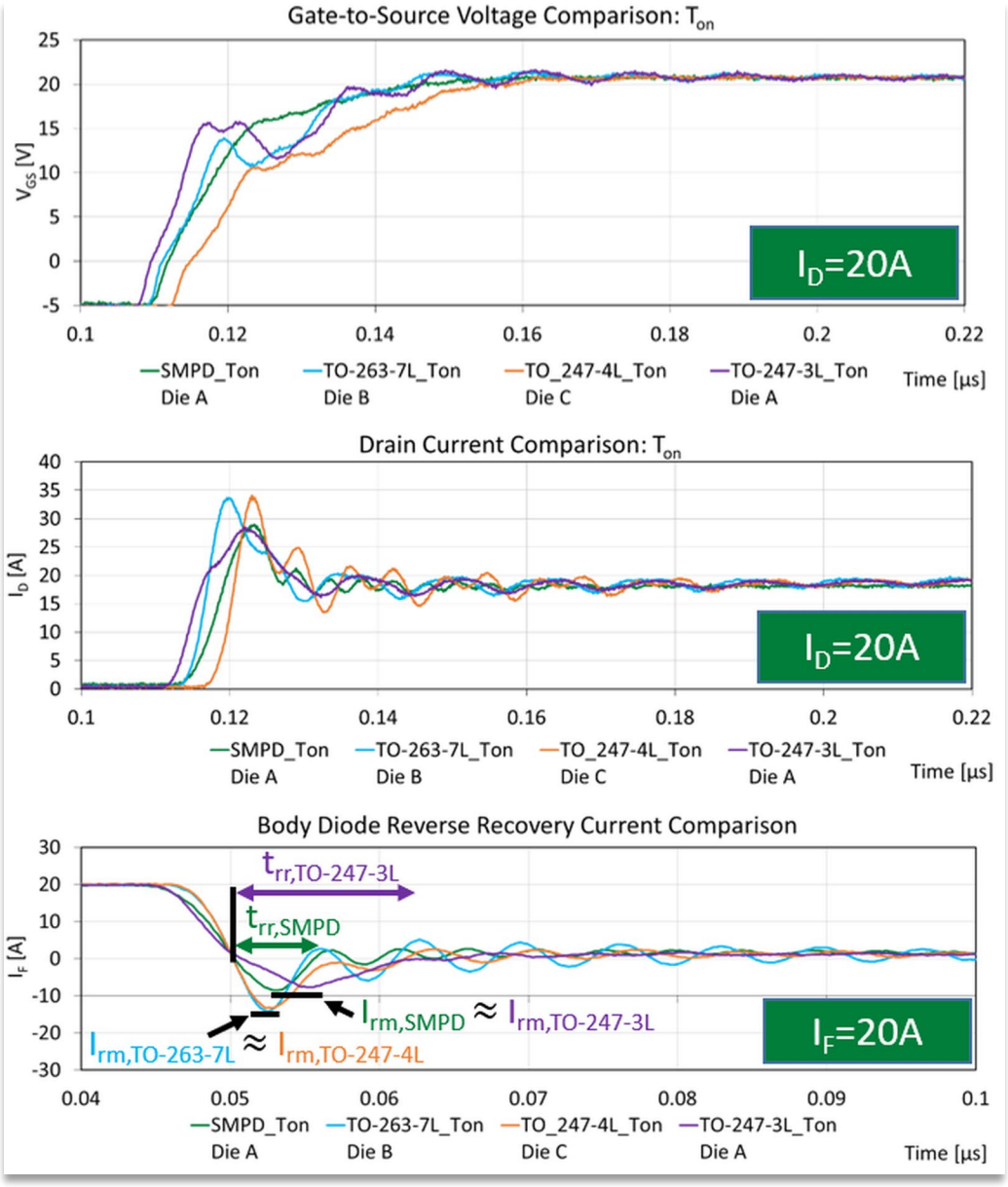

Figure 4. Waveform comparison between SMPD and standard TO-packages

As can be seen in **Figure 5**, the devices' dynamic behavior is quantified and illustrated in terms of percentage comparison. It can be concluded from the measurements that the SMPD offers a significant improvement in all aspects as compared to standard discrete packages. Despite having the same chip in the SMPD and the TO-247-3L package, the former offers significant performance improvements in application. For example, in an application with 80 kHz switching frequency and 800 V drain-source voltage, the SMPD is shown to offer a 21% reduction in switching losses for medium load conditions, and an 18% reduction under heavy load conditions. This indicates the SMPD loss reduction is more pronounced at medium loads when compared to all other discrete devices.

It is important to note that the performance of the TO-263-7L device is on par with the SMPD for heavy load conditions; however, using a TO263-7L package will usually require the use of an Insulated Metal Substrate (IMS) PCB. This restricts the number of PCB layers, adds complexity to the thermal management and to the PCB design, and generates a nearly 50% higher cost when compared to using a standard PCB. The SMPD, offering kelvin source connections and minimized package-level stray-inductance, optimizes performance, efficiency, and power density with any standard PCB. Additional benefits of using the SMPD include ease of manufacturing due to its standard reflow soldering capability.

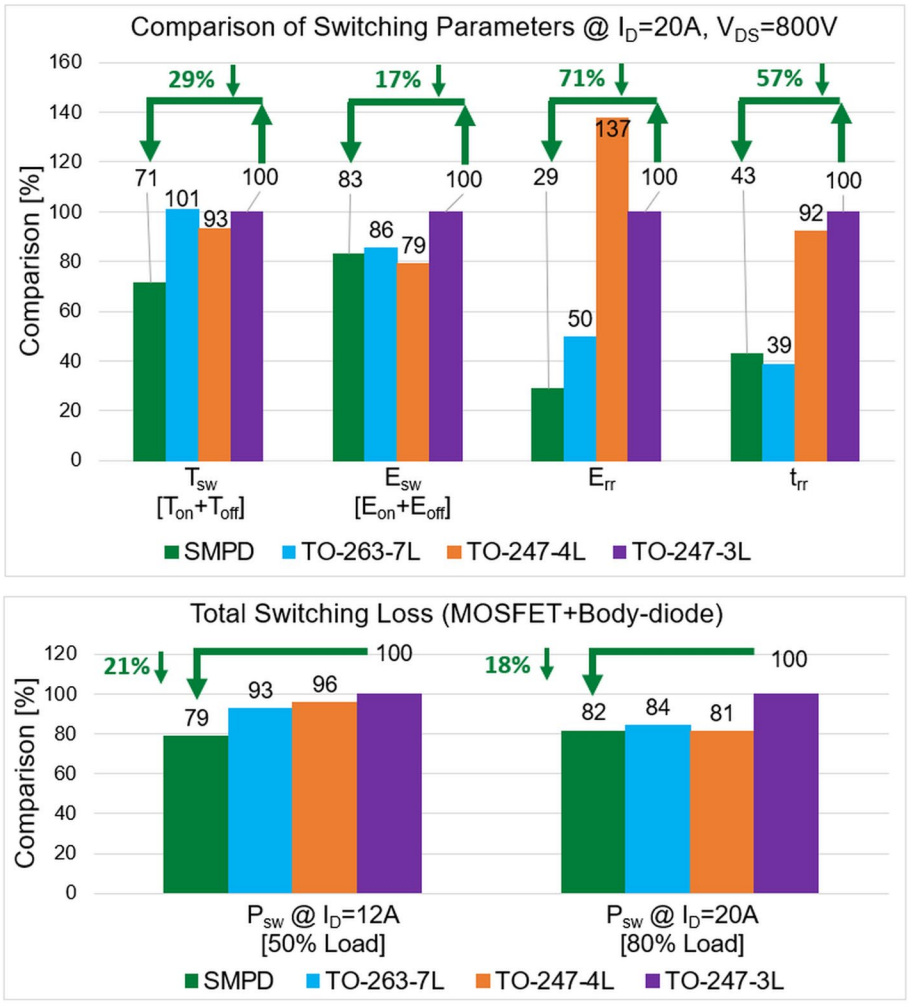

Figure 5. Comparison of relevant parameters between SMPD and standard discretes

3. Advantages of Using SiC-MOSFET-based SMPD in Applications

The depiction of an SMPD device mounted on a PCB with a standard load circuit is shown in **Figure 6**. Such a design approach provides the following benefits:

- Due to the kelvin source and separation of the gate drive path from the load circuit, no negative feedback of the load current goes into the gate loop. This improves the EMI performance and reduces the risk of parasitic turn-on.
- Most of the stray inductance, L_s, is excluded from gate loop, enabling faster switching, and reducing losses and gate oscillations.
- Minimized mutual parasitic inductance and coupling capacitance of the package yield optimal performance capability.
- Minimized losses improve efficiency and keep the junction temperature, T_{vj}, low, thus simplifying the thermal design.
- DCB-based fully isolated package requires reduced mounting and cooling efforts [3].

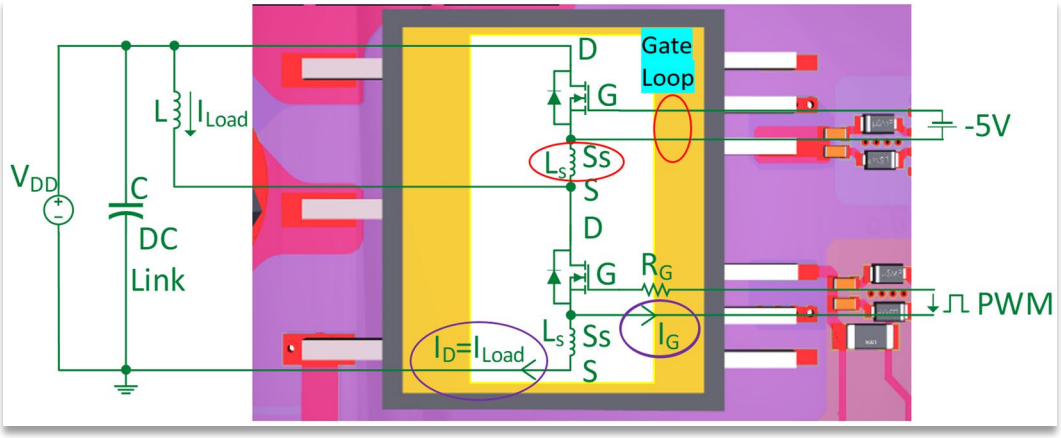

Figure 6. SMPD visualization with standard load circuit

By using the SMPD, designers can achieve shorter power loops while reducing the number of necessary components. The shorter power loop minimizes the stray inductance and mitigates gate ringing and drain voltage overshoots. An example of power loop optimization using a SMPD half-bridge versus using two standard TO-packages is illustrated in **Figure 7**.

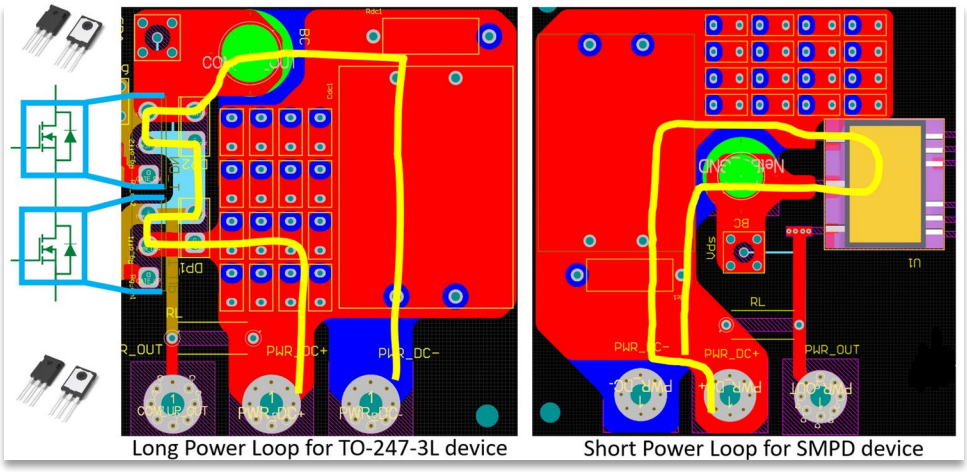

Figure 7. Shorter power loop with SMPD compared to standard discrete devices

4. Thermal Performance Comparison between SiC-based SMPD and Standard Discretes

Most of the standard discrete power semiconductor packages have an electrically conductive mounting tab. It is typically necessary to mount multiple discrete devices on the same heat sink frame, and to electrically isolate the devices' mounting tabs from the heat sink. A widely used approach in the industry is to insert a thermally conductive isolation foil between the semiconductor package and the heatsink. However, there are major penalties involved in using external isolation: increased junction-heatsink thermal resistance, R_{thJH}, reduced power and current handling capability, and complex thermal management with significant assembly efforts [4].

Reduced power handling capabilities are a major penalty in instances where wide band gap semiconductors such as SiC-MOSFETs are used, and where maximum performance is expected. A DCB-isolated SMPD improves the system's R_{thJH} and power-handling ability compared to standard discrete packages combined with thermally conductive isolation foil. Littelfuse has now developed SMPDs with high-performance ceramic which further reduces the junction-case thermal resistance, R_{thJC}, and junction-heatsink thermal resistance, R_{thJH}, as compared to alumina DCB-based SMPD. This helps to keep SiC-chips cooler at any given DC current. Thermal measurements incorporating 1200 V SiC MOSFET chips were conducted in three different packages, as shown in **Table 2**.

Table 2. Thermal measurement comparison of devices featuring SiC MOSFETs

	TO-247	SMPD	SMPD
Isolation	External, thermally conductive foil	Internal, alumina ceramic	Internal, high-performance ceramic
Sic Die	Same in all three packages		
$V_{(BR)DSS}$ (V)	1200	1200	1200
$R_{DS(on)25}$ (mΩ)	25	25	25
I_{D25} (A)	90	55	77
R_{thJC} (K/W)	0.27	0.7	0.45

Thermal impedance measurements were performed on each of the devices in two steps. First, a calibration curve was measured for all three devices. This was then used to determine the relationship between the temperature sensitive electrical parameter (TSEP) and the device temperature. For a SiC MOSFET, its body diode voltage drop, V_{SD}, having a linear relationship with the device's junction temperature, T_{vj} at a given measurement current, I_M serves as a TSEP. The measurement current, set to 100 mA, was assumed to be low enough to prevent self-heating of the chip, while simultaneously being large enough to maintain the desired measurement accuracy and noise immunity during transient thermal impedance measurements [5].

The general set-up for the calibration curve measurement is shown in **Figure 8**.

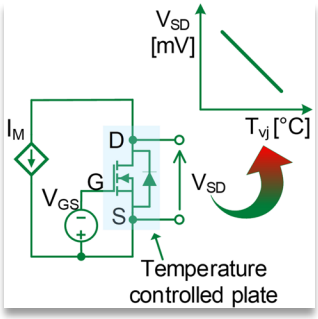

Figure 8.Calibration curve measurement principle

In the second step, the trend of transient thermal impedance, Z_{thJH}, and the junction temperature, T_{vj}, was determined using the cooling curve method in accordance with IEC 60747-8 [6].

The simplified test set-up for thermal measurement is depicted in **Figure 9**. The Device Under Test (DUT) is supplied with the heating current, I_H, for 15 s and then is switched to the measurement current I_M at time t=0 to let the DUT cool down for 180 s. During this cooling period, only I_M flows through the DUT. Thus, the linear relationship between V_{SD} and T_{vj} established during calibration measurements, can now be applied. The values of Z_{thJH} and T_{vj} for the DUT are then extracted with the help of the calibration coefficient obtained from the calibration measurement.

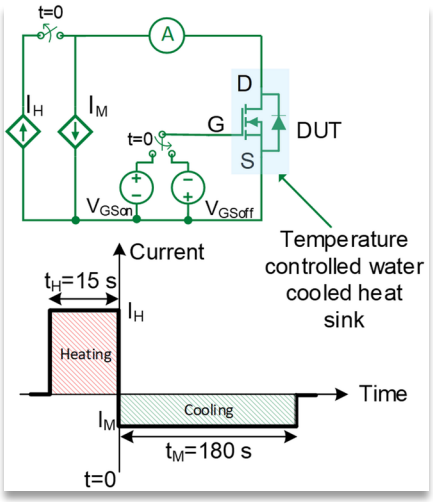

Figure 9.Thermal impedance measurement principle

For the thermal measurements, the TO-247 device was assembled with two different external isolation foils with thermal conductivity of respectively 4.5 W/mK and 6.5 W/mK between the package and the heatsink, to imitate a real-world application. The SMPD device used thermal paste between the package and the heat sink while holding the phase leg configuration of 25 mΩ SiC MOSFET chips inside. During the thermal measurements on the SMPD, only one SiC chip was measured while the other chip was kept inactive. The devices were mounted on temperature-controlled, water-cooled heatsinks with a constant temperature of 30°C. Thermal measurement results for the 25 mΩ SiC MOSFET chip at I_H = 40 A in different packages are illustrated in **Figure 10** and **Figure 11**.

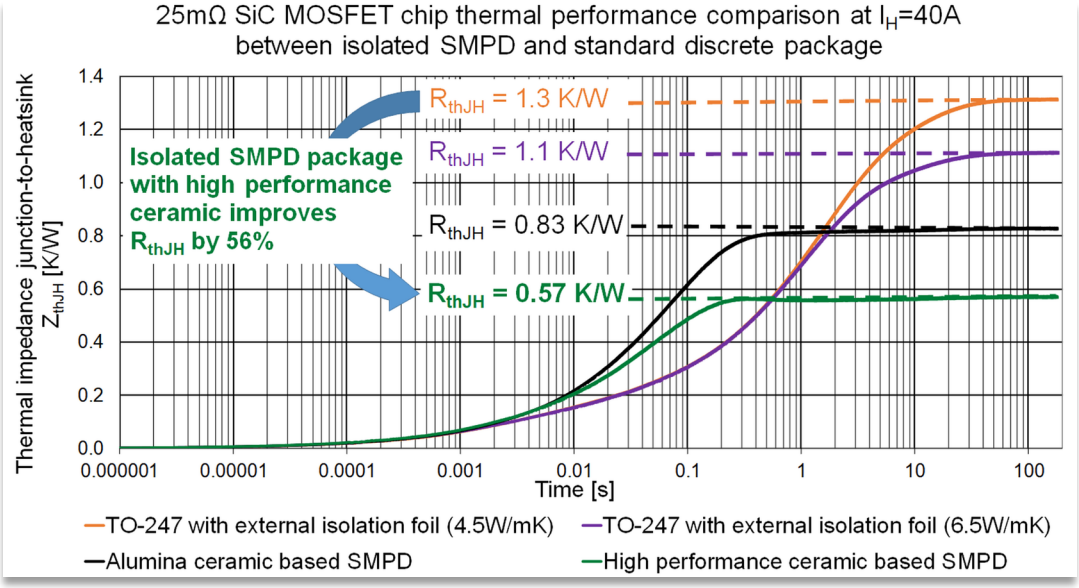

Figure 10.Thermal impedance measurement comparison between SMPD and TO-247 discrete

As evident from **Figure 10**, the SMPD with high performance ceramic improves the steady state thermal resistance, R_{thJH}, by 56% when compared to the TO-247 with the same chip. This directly translates into increased power handling and lower chip temperature at the given drain current. As depicted in **Figure 11**, the SiC chips in the SMPD package with improved ceramic stay up to 75°C cooler when compared to the TO-247 device with external isolation at I_H = 40 A. This results in a lower temperature swing between the junction and heatsink, ΔT_{JH}, at the given heating power. The SMPD with a high-performance ceramic has an almost 58% reduction in temperature swing ΔT_{JH} compared to the standard discrete, significantly improving the device's lifetime and in turn the reliability of the application.

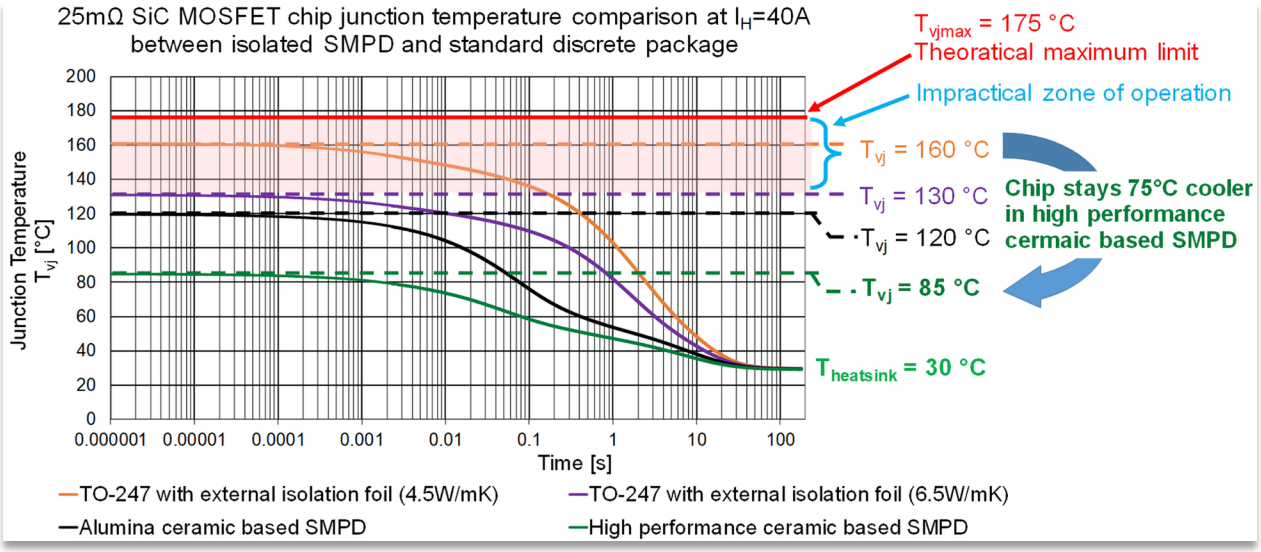

Figure 11. Junction temperature comparison between SMPD and TO-247 discrete

It is also worth mentioning that the practical zone for T_{vj} within the application is usually up to 130°C to ensure safe operation. By comparing the SMPD's performance to the TO-247 with 6.5 W/mK foil in **Figure 10** and **Figure 11**, it is visible that the SMPD with high performance ceramic improves thermal resistance, R_{thJH}, by 48% and offers a 45% lower temperature swing, ΔT_{JH}. Compared to conventional alumina ceramic-based SMPD, the high-performance ceramic-based SMPD offers 30% lower R_{thJH} and 40% lower temperature swing, ΔT_{JH} with the same SiC chip.

5. Increasing Application Power Output with SMPD

During thermal measurements, the heating current, I_H, which results in a chip temperature, T_{vj}, of 130°C was measured for different packages embedding the same 25 mΩ SiC chip. Thermal measurement results have been summarized in **Table 3**. Real-world applications are usually designed to work at 130°C chip temperature; therefore, the result can be interpreted in terms of application advantages. The SiC chip in the TO-247 package combined with an external isolation foil reached 130°C junction temperature at 37.7 A drain current. This is only 40% of the chip's rated I_{D25} value. The same SiC chip in the SMPD with high performance ceramic reached 130°C at 48.4 A drain current. This is almost 50% of the chip's rated I_{D25} value. The SMPD with improved ceramic could sustain 130% higher power dissipation junction-heatsink, P_{DJH}, when compared to the standard discrete solutions.

Table 3. Thermal measurement results at T_{vj} = 130°C

	T_{vj} (°C)	I_H (A)	R_{thJH} (K/W)	P_{DJH} (W)
TO-247 with 4.5 W/mK isolation foil	130	37.7	1.31	77
TO-247 with 6.5 W/mK isolation foil	130	40	1.11	91
Alumina ceramic-based SMPD	130	41.4	0.83	122
High-performance ceramic-based SMPD	130	48.4	0.57	177

These measurements show that the SMPD with improved ceramic takes 28% higher current to reach a chip temperature of 130°C. Considering an 18 kW application designed with 25 mΩ SiC MOSFET in TO-247 package utilizing the 4.5 W/mK external thermal foil and assuming to work with a 800 V DC-link, the DC power output of this application can be potentially increased up to 26.6 kW by using an SMPD with improved ceramic, translating into a possible 48% increase in DC power output, as depicted in **Figure 12**.

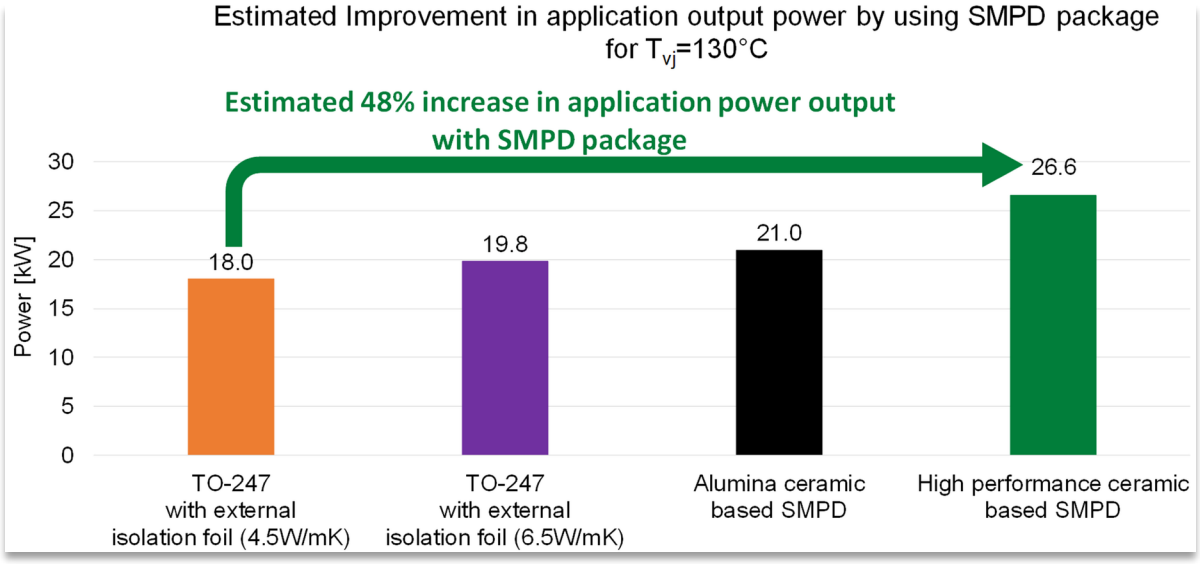

Figure 12. Estimated increase in application power output by using SMPD

6. System-level Cost Saving Opportunity by using SMPD

The standard TO-package with external thermally conductive isolation foil severely restricts the application power output capability due to poor thermal resistance, R_{thJH}. Consider a 20 kW application having a 800 V DC-link voltage, designed with latest generation 18 mΩ SiC MOSFETs in TO-247 and external isolation foil. Using the SMPD package with high performance ceramic in the same application, it could be possible to achieve the same power output level with the latest generation 36 mΩ chip due to the improved thermal performance. This results in significant cost saving at a system level. The potential cost saving opportunity offered by SMPD as compared to a conventional discrete solution is summarized in **Table 4**.

Table 4. Cost saving opportunity per MOSFET device by using SMPD in applications

Cost Savings	Amount (US $)
Cost saving per MOSFET chip	4
Cost saving per MOSFET assembly (isolation foil, labor, mounting)	2
Cost saving in discrete package heatsink, screw, and washer	2
Total Cost Savings per MOSFET	**8**

Note: Not considered in the calculation above are further potential cost savings due to:
– Volume production of SMPD-based PCBs using automation and standard reflow soldering
– Cost saving in isolation cutting tool (one time $700)
– Reduced potential warranty claims due to performance and reliability degradation of isolation foil for discrete
– Decrease in component count and space saving in application using SMPD

7. Summary

By comparing the electrical performance of Littelfuse SMPD with standard TO-247 discrete embedding SiC MOSFET chips, the SMPD-based design was shown to offer a significant reduction in MOSFET switching and body diode losses, improving the overall application efficiency. From thermal measurement comparison between SMPD and TO-247 discrete, it was established that an SMPD with a high-performance ceramic reduces the thermal resistance R_{thJH} by 56%, temperature swing ΔT_{JH} by 58%. The SiC MOSFET chip in the SMPD package therefore stays up to 75°C cooler at the same DC output power. This improves the overall device's lifetime and application reliability. Considering an 18 kW application example, the SMPD offers the possibility of increasing application power output by 48%. In other words, for a given application power rating, it is possible to design-in higher $R_{DS(on)}$ chips due to improved thermal resistance R_{thJH} and power dissipation P_{DJH} of the SMPD package with high performance ceramic.

These advantages create significant cost-saving opportunities at the system level. Approximate calculations show a potential cost saving opportunity of up to US $8 per MOSFET device when using an SMPD in place of a standard discrete solution. The usage of SMPD in power electronic applications provides internal isolation, reduces mounting efforts, enables space saving, reduces overall thermal resistance, and increases power density and efficiency along with simplified thermal design.

8. References

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