Dynamic Characterization Platform

Objectives

The Dynamic Characterization Platform from Littelfuse is designed to:

- Measure:
  - MOSFET switching losses, switching times, and gate charge accurately
  - Schottky Barrier Diode (SBD) and body diode reverse recovery accurately
- Provide an informed reference design for gate drive and power loop PCB layout.
- Provide informed recommendations for gate drive layout and components.
- Promote streamlined device validation and quicker design cycles.

Target Audience

The Dynamic Characterization Platform (DCP) enables design engineers to characterize the high performance Silicon Carbide (SiC) MOSFETs and diodes offered by Littelfuse with high accuracy. Functionality highlights of this evaluation kit include:

- Designed for TO-247-3L SiC MOSFETs and TO-220-2L SiC Schottky Barrier Diodes
- Power loop and gate drive circuitry optimized for ultra-fast dV/dt and dI/dt events
- Integrated input signal and measurement probe interface connections

Contact Information

For more information about this evaluation kit, including design files, please visit our SiC products web page at: http://www.littelfuse.com/products/power-semiconductors/ silicon-carbide.aspx.

For further technical details about the Dynamic Characterization Platform, please contact our SiC Application Support Hotline, powersemisupport@littelfuse.com

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1. Introduction

High voltage Silicon Carbide MOSFETs and diodes have fast switching speeds and very low switching losses. This enables power converters to be operated at higher frequencies when compared to traditional power converters that use silicon devices. Higher operating frequencies and very low switching and conduction losses lead to multiple system-level optimization opportunities, including power converters with higher efficiency and power density. Reduction in magnetics size and simpler thermal management designs can also lead to total system cost reduction. Although previous generations of power converters were limited by the switching speed and high losses of high voltage silicon switches, new fast switching and low loss SiC MOSFETs and diodes all but eliminate this constraint and provide designers with the opportunity to redesign compact, super-efficient power converters with low cost.

Although SiC MOSFETs behave much like silicon MOSFETs and are quite simple to drive, designers must pay special attention to certain aspects in order to harness the full advantage of these fast switching devices. The switching behavior of the MOSFETs can be severely impaired by parasitic inductances stemming from poor PCB layouts. These parasitic inductances, coupled with the fast dV/dt and dI/dt characteristics of the SiC MOSFETs, can lead to a number of undesirable effects, including voltage and current overshoot, increased switching losses, and system instability. Additionally, using traditional silicon IGBT-based techniques to characterize the switching behavior of SiC MOSFETs may result in erroneous conclusions about switching losses due to issues such as insufficient measurement probe bandwidth and equipment inadequacy.

The Dynamic Characterization Platform (DCP) from Littelfuse is designed to characterize SiC MOSFET and diode switching losses via the double-pulse technique. It can also be used to characterize other typical dynamic parameters provided in MOSFET and diode datasheets, such as switching times, gate charge, and reverse recovery. As previously mentioned, measuring these parameters for SiC devices requires an optimized board layout and precise voltage/current sensing techniques. To begin implementing good SiC device characterization practices, please visit our website and download the DCP reference design package, which contains schematic, board layout, and Bill of Materials files, along with this application note.

Table 1. Classification Temperature (T_c) for Pb-free Solder Process

Electrical Specifications			
Parameter	**Typical Value**	**Maximum Rating**	**Units**
Input DC Link Voltage	800	1000	V
Input Control Voltage	12	13.2	V
Output Peak Current	-	100	A
Ambient Temperature	-	55	°C
Gate Driving Voltage	+20/ -5	+22/ -6	V

2. Overview

Figure 1 is a block diagram of the Dynamic Characterization Platform. It is arranged in a single-phase leg configuration that accommodates two SiC MOSFETs and optional anti-parallel Schottky diodes. Each MOSFET has its own gate driver circuit, including individual digital isolators, current boosters, and isolated power supplies.

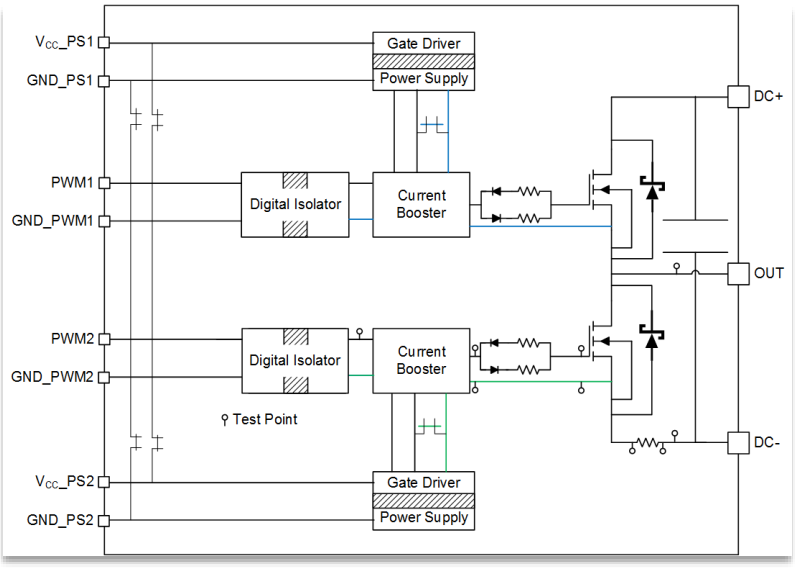


Figure 1. Block Diagram of the Dynamic Characterization Platform

The DCP includes three high-voltage power connections (DC+_ Con2, DC-_Con1 and OUT_Con3), two pairs of low-voltage connections for gate driver control circuitry (VCC_PS1/GND_PS1 and VCC_PS2/GND_PS2), two BNC terminals for gate signals (PWM1/GND_PWM1 and PWM2/GND_PWM2), and one 8-pin header that can be used as an alternative interface for the gate signals (not shown in Figure 1).

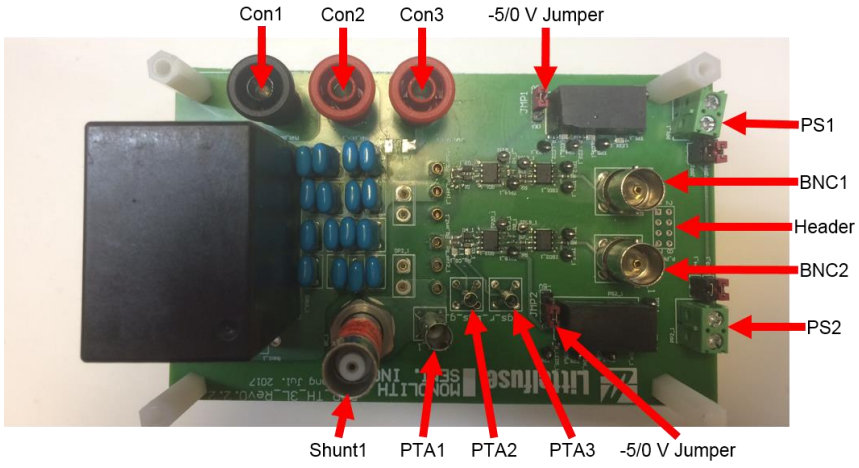


Figure 2. Interface Connections for Dynamic Characterization Platform

Each switch position's gate driver circuitry features a Silicon Labs digital isolator [Si8261], an IXYS current booster [IXDN614], and a Murata 2W isolated DC-DC converter [MGJ2D122005SC]. The Murata DC-DC converter uses a +12 V input to generate +20 V and -5 V rails with a 5.2 kV DC isolation barrier. The negative driving voltage can be configured (-5 V or 0 V) via a 100-mil header jumper. The gate loop is separated into two (diode + 0603 SMD resistor) legs to allow for different turn-on and turn-off gate resistances. The on-board probe-tip adapters (PTAs) improve measurement accuracy for gate-source voltage (VGS) and drain-source voltage (VDS). A coaxial current viewing resistor shunt is used for accurate switching current measurement. High-voltage DC link capacitors are provided in the form of one larger film capacitor (which stabilizes the DC bus during switching transients) in parallel with multiple smaller ceramic capacitors (which provide a decoupling function for current commutation between devices). A phase leg configuration that includes accommodations for two SiC MOSFETs and optional anti-parallel Schottky diodes supports testing either MOSFETs or diodes. The socket mounting method for the MOSFETs and diodes allows for fast and easy swapping of DUTs. Likewise, high-voltage banana connectors are used for convenient power connections. An on-board through-hole resistor can be mounted for resistive load testing; an external load inductor is needed for inductive load pulse testing.

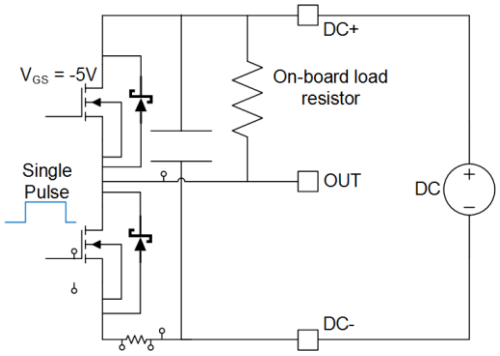
Figure 3. Dynamic Characterization Platform Assembly

The dimensions of the DCP (Figure 3) are 132 mm x 86 mm. It is designed to perform pulse testing only, so no device cooling accommodations are provided. This board is designed to test MOSFETs in 3-lead TO-247 packages and diodes in 2-lead TO-220 packages. Custom DCPs for other through-hole packages and SMD packages can be developed on request.

3. Configurations

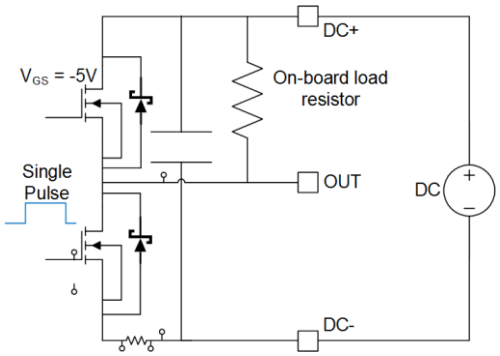
The DCP has the flexibility to implement several important SiC device characterization test circuits, including resistive load single-pulse testing for switching time behavior, inductive load double-pulse testing for switching energy/time behavior and gate charge behavior, and inductive load double-pulse testing for reverse recovery behavior.

The possible topologies for different tests are summarized below. Switching tests can be performed with or without anti-parallel SBDs. The free-wheeling device can be implemented via a single SBD, a single MOSFET (with body diode), or a combination of an SBD and a MOSFET in parallel with one another, as shown in the schematics in Figure 4, Figure 5, and Figure 6.



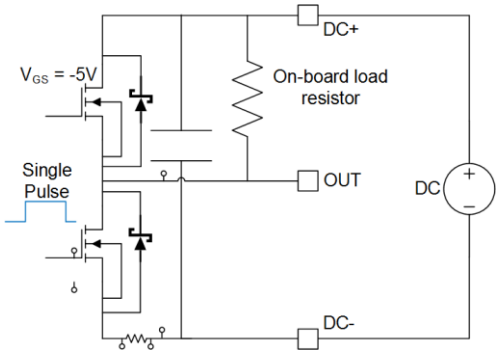
- Single-pulse test
- Test switching behavior of switching MOSFET with resistive load (delay time, rise/fall time)
- Resistive load implemented via on-board through-hole resistor

Figure 4. Resistive Load Test



- Double-pulse test
- Test switching behavior of switching MOSFET with inductive load
- Test gate charge behavior of MOSFET
- Selective MOSFET or diode for free-wheeling device
- Inductive load implemented via off-board load inductor

Figure 5. CIL MOSFET Switching Loss Test



- Double-pulse test
- Test reverse recovery behavior of free-wheeling devices
- Selective MOSFET or diode for free-wheeling device
- External load inductor needed

Figure 6. Reverse Recovery Test

4. Hardware Description

4.1. Key Components and Connectors

4.1.1. Device Under Test (DUT)

This Dynamic Characterization Platform can characterize the switching behavior of the switching devices and the free-wheeling devices in a half-bridge configuration. For switching device characterization, the DUT can be implemented as a MOSFET only or as a MOSFET with an external anti-parallel diode. For free-wheeling device characterization, the DUT can be implemented as a single free-wheeling diode, a MOSFET with body diode, or a MOSFET with body diode and an additional free-wheeling diode in parallel.

4.1.2. DC Link Capacitor and Decoupling Capacitor

Decoupling capacitors provide energy during device switching. DC link capacitors stabilize DC link voltage during switching transients. The decoupling capacitors and DC link capacitor in the DCP together form a low-pass filter that filters the switching current on the DC bus. This reduces the impact of any parasitic inductance related to the wire connection between the DC source and the on-board DC bus of the test system.

4.1.3. Free-wheeling Device

When the bottom switch position MOSFET is turned off in a double-pulse test, a current path is required for the energy stored in the off-board inductor to circulate through. This is accomplished by inserting a semiconductor element that limits current flow to one direction in parallel with the inductor. The semiconductor element is commonly composed of a SiC SBD, SiC MOSFET with body diode, or a SiC MOSFET and SiC SBD in parallel. These configurations represent common, real-world configurations seen in a buck or boost converter with an SiC SBD diode for the free-wheeling device. Another common configuration appears in a half-bridge topology, where the need for a free-wheeling device is satisfied by the body diode of the SiC MOSFET.

4.1.4. Isolated Power Supply

Implemented in the gate driver circuitry, this component provides an isolation barrier for logic signals.

4.1.5. Current Viewing Shunt Resistor (Rshunt)

A coaxial type shunt resistor offers the optimal solution for measuring the device current. The coaxial shunt allows making a high bandwidth measurement while introducing only a minimal amount of parasitic inductance into the power loop of the testing circuit. For details of the coaxial shunt, refer to T&M Research® (SSDN-414 series, 50 mΩ with 2000 MHz bandpass frequency and 0.18 ns rise time). The output of the CVR is directly connected to the oscilloscope via a 50 Ω terminator and an RG58 BNC cable.

4.1.6. Voltage Measurement Probes

Passive probes are recommended for drain-source voltage and gate-source voltage measurements. High bandwidth, low input impedance, and proper de-skewing between voltage and current measurements are necessary for accurate switching loss measurements. Probe-tip adapters are provided for convenient PCB to probe-tip interface connections and optimized voltage measurement.

4.1.7. Off-board Load Inductor

Here are some important tips for selecting a proper off-board inductor:

- Avoid saturation at target device current.
- Ensure enough inductance so that the turn-off and turn-on events will have similar current.
- Larger inductance will allow for easier and more accurate programming of device current.
- Avoid paralleling of multiple inductors, which would result in higher equivalent parallel capacitance and potential for LC resonant ringing during a switching event.

4.1.8. Signal and Power Connection

Input PWM signals should be controlled with a 3.3 V signal via BNC1 and BNC2. Gate drive power supply input voltage should be 12 V, applied via PS1 and PS2.

4.2. Connector Definitions

The board (Figure 3) has three power connections: Con1 is for negative DC bus input, Con2 is for positive DC bus input, and Con3 is the mid-point of the phase leg. PS1 and PS2 are for the +12 V power supply input for the gate driver control circuitry. BNC1 and BNC2 are gate signal input connection terminals for the function generator. The Header connector provides an alternative gate signal input option for digital controllers. The definition of the Header connector is shown in Table 2.

Table 2. Header Connector Pin Definitions

Pin	Definition
1	PWM1
2	GND_PWM1
3	NC
4	NC
5	NC
6	NC
7	PWM2
8	GND_PWM2

For measurements, three probe-tip adapters (PTAs) are implemented with measurement loop reduction in mind. PTA1 is for the drain-source voltage (V_{DS}) measurement. PTA2 is for the gate-source voltage (V_{GS}) measurement. PTA3 is for the measurement of the gate signal before gate resistor (used during gate charge measurement tests). Shunt1 is the BNC connection for the switching current (I_{DS}) measurement.

4.3. Gate Drive Loop and Power Loop Design

SiC devices switch extremely fast, so it is important to minimize the voltage overshoot and current ringing during switching transients. A common contributor to ringing seen during switching events is the loop inductance in the semiconductor packaging and PCB layout design. Figure 7 shows some key sources of parasitic inductances in a half-bridge configuration.

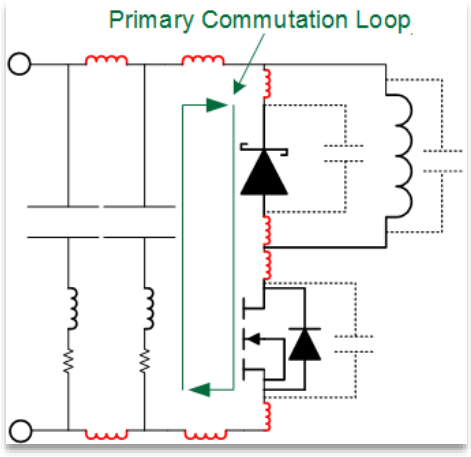


Figure 7. Key Stray Inductance Sources in Half-Bridge Configuration

The DCP uses design approaches that optimize both power loop and gate loop design to minimize loop inductance and cross coupling. Here are some of these design guidelines:

- The current booster should be placed as near as possible to the gate pin of the SiC MOSFET to reduce the length of the gate path. The source pin of the MOSFET should be connected to a copper ground plane on the PCB directly beneath the gate path. This results in the gate loop being minimized in such a way that only the thickness of the PCB contributes to the gate loop size.
- Additional decoupling capacitors for the current booster ICs are recommended. These decoupling capacitors should also be placed as near as possible to the gate of the MOSFET to reduce the gate loop.
- DC link decoupling capacitors are necessary to reduce the drain-source voltage ringing during switching. Multiple small decoupling capacitors in parallel are recommended to reduce parasitic inductance of each capacitor. The decoupling capacitors should also be placed as near to the SiC MOSFETs as possible.
- A laminated DC bus structure is recommended to reduce DC bus inductance. For that reason, it is better to use copper planes than traces for the DC positive and DC negative bus signals. Furthermore, these planes should reside on different PCB layers and overlap with each other to form the laminated DC bus structure.
- The placement of the two MOSFETs and their anti-parallel diodes should be carefully considered to ensure a small current commutation loop between the top device and bottom device.

4.4. Load Inductor Selection

To collect accurate switching loss measurements, the load inductor must be chosen carefully. The load inductor should have low equivalent parallel capacitance (EPC) compared to the output capacitance of the DUT. Selecting a load inductor that has an EPC smaller than 10 pF is recommended when testing 1200 V, 80 mΩ SiC MOSFETs from Littelfuse. Another important quality of the load inductor is that it should not be saturated at the target turn-off/turn-on current. For internal testing purposes, Littelfuse leverages four high current encapsulated inductors [EK55246-341M-40AH] from Coil Winding Specialist, Inc. These have been custom packaged in enclosures with banana jack interface terminals that allow for quick and easy configuration depending on testing needs (e.g., low current + high inductance or high current + low inductance operation).

Figure 8. Load Inductor Example

5. Example Application and Measurement

5.1. Test Setup

Figure 9 shows the block diagram schematic of a double-pulse test setup. In this test, an inductive load is placed in parallel with a free-wheeling diode (FWD) in the upper switch position. These elements make up the free-wheeling path for current during DUT turn-off states. The DUT occupies the lower switch position. This testing configuration is used to study switching energy and gate charge characteristics of the DUT.

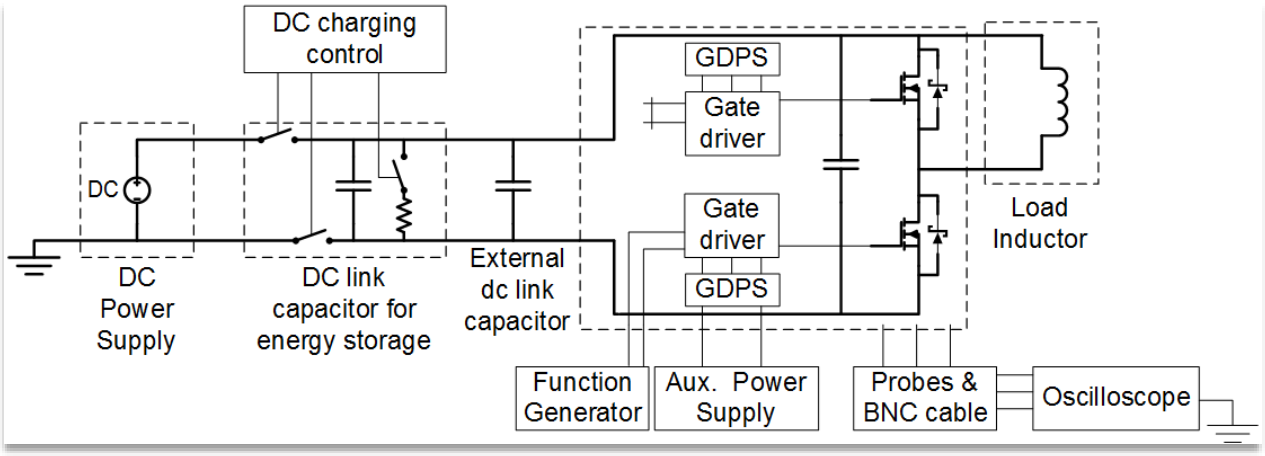


Figure 9. Test Setup Schematic

Note: The measurement equipment and the DC power supply each have their own connection to earth ground. To prevent a ground loop that may cause significant measurement error, isolating the DCP galvanically from the DC power supply during tests is recommended while measurements are being collected. In this test system, voltage controlled relays [P105] from GIGAVAC are used for disconnecting the DC power supply (positive and negative rails) from the DCP. The DC link capacitance is sized so that it can maintain the desired bus voltage throughout the test after being disconnected from the DC power supply. This improves measurement conditions by minimizing the risk of ringing during transient events caused by ground loops. If the system does not have accommodations for a sufficiently sized DC link capacitor that allows for disconnection from the DC voltage supply as described above, the system still requires, at minimum, a DC link capacitance of sufficient size to maintain DC voltage during device switching. Refer to the appendix for additional details regarding required peripheral equipment.

5.1.1. Measurement Details

The high switching speed of SiC MOSFETs means the dv/dt and di/dt may exceed 80 V/ns and 5 A/ns respectively under certain test conditions. These devices are switching on and off within tens of nanoseconds. Therefore, it is critical that the measurement probes have adequate bandwidth, good dynamic performance, and very small loading capacitance. For testing with the DCP, passive voltage probes are recommended for V_{DS} and V_{GS} measurements. A current viewing resistor shunt is recommended for the I_{DS} measurement.

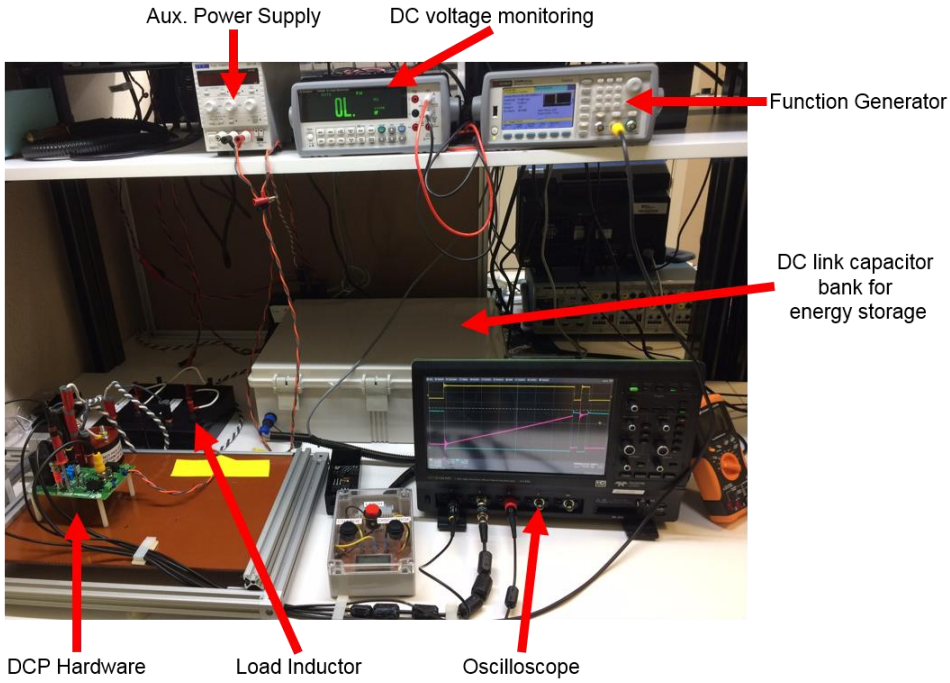


Figure 10. Test Setup

For this example, a current viewing resistor (CVR) from T&M Research (SSDN-414-05) is used to measure I_{DS}. This model's specifications include a 2 GHz bandwidth and 0.18 ns rise time. The output of the CVR is directly connected to the oscilloscope via a 50 Ω terminator and an RG58 BNC cable. Note: The settings for the oscilloscope's channel used for this measurement should be configured to reflect a 50 Ω termination.

For the V_{DS} measurement, a probe-tip adapter is provided on the DCP PCB that accommodates the 400 MHz bandwidth, high-voltage passive probe [PPE4KV] from Lecroy. For the V_{GS} measurement, a probe-tip adapter is provided on the DCP PCB that accommodates the 500 MHz bandwidth, low-voltage passive probe [PPE023] from Lecroy. If other voltage probes are used, the user should ensure that the probes have ≥400 MHz bandwidth and sufficient voltage margin for the signal to be measured. If the probe-tip adapter does not match with the probe in use, the user has the option to replace the probe-tip adapter with an SMA connector and an SMA to probe-tip adapter.

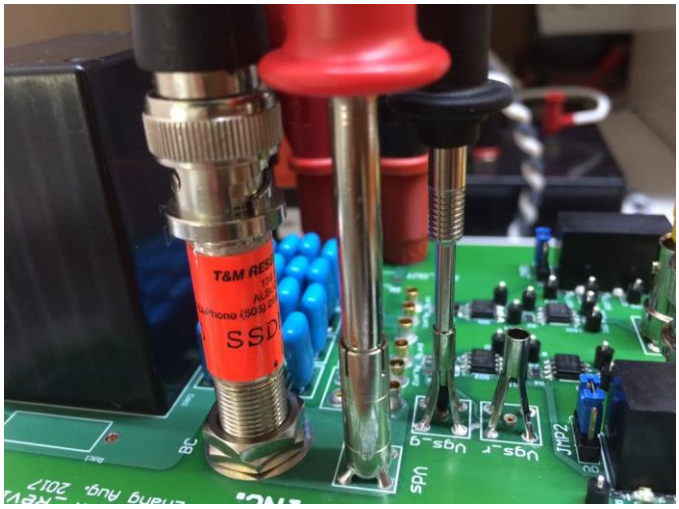


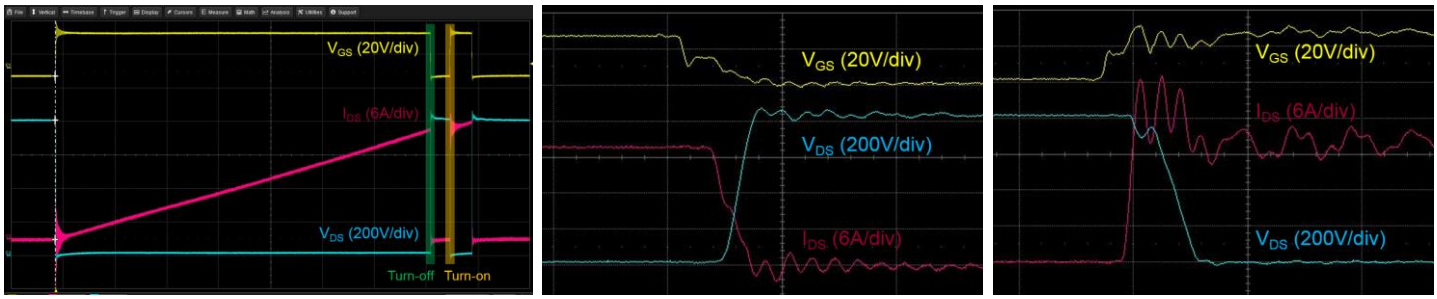
Figure 11. Probe-tip to PCB Interface Connections

In addition to adequate probes, a high-performance oscilloscope should also be used to ensure accurate voltage and current measurements. The minimum recommended specifications for the oscilloscope are:

- Bandwidth ≥ 400 MHz
- Sample rate ≥ 2.5 GS/s

5.1.2. Test Results

Figure 12 presents results for a test performed with an 800 V DC bus voltage and a device current of 20 A. In this figure, the gate-source voltage (V_{GS}), drain-source voltage (V_{DS}), and device current (I_{DS}) are shown. Sub figures (b) and (c) show magnified portions of the waveforms from (a) that correspond to the turn-off (b) and turn-on (c) events. These events are used to characterize the switching behavior of the MOSFET in detail by describing its switching energy, switching speed, rise and fall times, voltage overshoot, etc.



(a) Double-pulse Test Captured Waveforms (10 µsec/div) | (b) Turn-off Transient Waveforms (50 nsec/div) | (c) Turn-on Transient Waveforms (50 nsec/div)

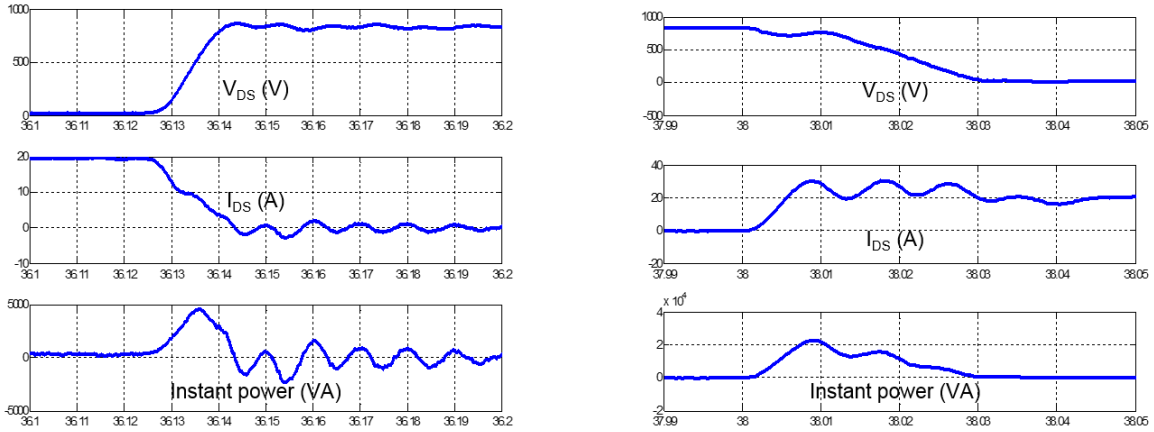
Figure 12. Oscilloscope Screen Captures of Double-pulse Test Waveforms

5.2. Post-processing of Test Data

To obtain numerical values for the devices' switching characteristics, a certain amount of post processing must be done. MATLAB® is a useful software tool for handling these heavy computational load calculations. After importing the raw data into the post-processing environment, the next step is to ensure the drain-source voltage (V_{DS}) and device current (I_{DS}) are properly de-skewed. The switching loss results are highly sensitive to this step, so it is critical to the process; otherwise, results may be skewed by a significant percentage.

There are two ways to ensure the channels are properly de-skewed. The first way, a hardware de-skew, is performed by connecting the two channels used to measure the V_{DS} and I_{DS} signals to the same voltage signal/reference on the oscilloscope and adjusting the channel delay settings accordingly until the waveforms align with each other. Note: The connections from the oscilloscope channels to the oscilloscope voltage signal/ reference should be made with the probes (HV voltage probe for V_{DS} and BNC cable for I_{DS}) that will be used in the tests to ensure proper compensation. This method should always be the first step to ensuring proper de-skewing of the oscilloscope channels. A software de-skew can be performed as a way to check the accuracy of this hardware de-skew. This method involves first plotting the V_{DS} and I_{DS} current waveforms, both with respect to time. During the turn-off event, the V_{DS} signal should first cross the DC bus voltage set point (e.g., 800 V in this example) at the same time as the device current first crosses 0 A. If these instances occur at the same time, the hardware de-skew was successful and no further action is necessary. If the events occur at slightly different times, a manual shift of one waveform (V_{DS} or I_{DS}) along the time axis can be performed to align the two events previously discussed.

Figure 13 presents an example of plots generated with MATLAB for the turn-on and turn-off transient voltage (V_{DS}), current (I_{DS}), and instantaneous power after a proper oscilloscope channel de-skew. From these waveforms, switching energy calculations and switching behavior of the DUT can be derived.



(a) Turn-off Transient Waveforms

(b) Turn-on Transient Waveforms

Figure 13. MATLAB Processing of Double-pulse Test Waveforms

The waveforms shown in Figure 13 indicate that, during the turn-off event, a voltage overshoot of ~70 V is present, dv/dt = 68.72 V/ns, di/dt = 1 A/ns, and turn-off loss is ~60 µJ; during the turn-on event: a current overshoot of ~10 A is present, dv/dt = 39.47 V/ ns, di/dt = 5.2 A/ns, and turn-on loss is ~270 µJ.

Note: Switching loss values are obtained via integration of instantaneous power.

6. Reference

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7. Appendix

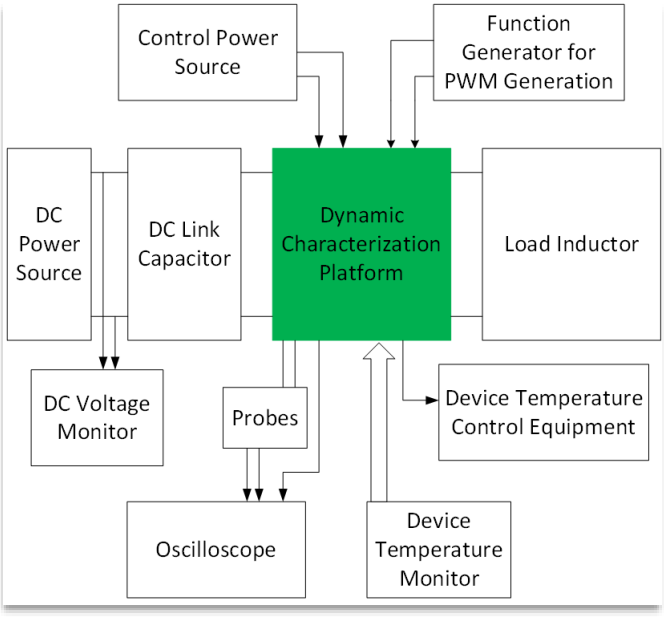

Figure 14. Peripheral Equipment

7.1. Design Files

For detailed PCB schematic and layout files, please visit: http://www.littelfuse.com/products/power-semiconductors/silicon-carbide.aspx.