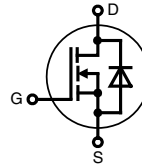


CoolMOS™ 1) Power MOSFET in ISOPLUS247™ Package

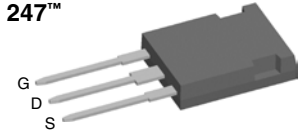
N-Channel Enhancement Mode
Low $R_{DS(on)}$, High V_{DSS} MOSFET
Package with Electrically Isolated Base



$$I_{D25} = 25 \text{ A}$$

$$V_{DSS} = 800 \text{ V}$$

$$R_{DS(on)} = 125 \text{ m}\Omega$$

ISOPLUS 247™


G = Gate, D = Drain, S = Source

MOSFET			
Symbol	Conditions	Maximum Ratings	
V_{DSS}	$T_{VJ} = 25^\circ\text{C to } 150^\circ\text{C}$	800	V
V_{GS}		± 20	V
I_{D25}	$T_C = 25^\circ\text{C}$	25	A
I_{D90}	$T_C = 90^\circ\text{C}$	18	A
dv/dt	$V_{DS} < V_{DSS}; I_F \leq 17 \text{ A} \mid di_F/dt \mid \leq 100 \text{ A}/\mu\text{s}$ $T_{VJ} = 150^\circ\text{C}$	6	V/ns
E_{AS}	$I_D = 4 \text{ A}; L = 80 \text{ mH}; T_C = 25^\circ\text{C}$	0.67	mJ
E_{AR}	$I_D = 17 \text{ A}; L = 3.3 \text{ mH}; T_C = 25^\circ\text{C}$	0.5	mJ

Symbol	Conditions	Characteristic Values			
		$(T_{VJ} = 25^\circ\text{C}, \text{ unless otherwise specified})$			
		min.	typ.	max.	
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}; I_D = I_{D90}$		125	150	m Ω
$V_{GS(th)}$	$V_{DS} = 20 \text{ V}; I_D = 2 \text{ mA}$	2		4	V
I_{DSS}	$V_{DS} = V_{DSS}; V_{GS} = 0 \text{ V}; T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$		100	50	μA μA
I_{GSS}	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0 \text{ V}$			200	nA
Q_g	$V_{GS} = 10 \text{ V}; V_{DS} = 640 \text{ V}; I_D = 34 \text{ A}$		180	355	nC
Q_{gs}			24		nC
Q_{gd}			92		nC
$t_{d(on)}$	$V_{GS} = 10 \text{ V}; V_{DS} = 640 \text{ V}$ $I_D = 34 \text{ A}; R_G = 2.2 \Omega$		25		ns
t_r			15		ns
$t_{d(off)}$			72		ns
t_f			6		ns
V_F	(reverse conduction) $I_F = 12.5 \text{ A}; V_{GS} = 0 \text{ V}$		1	1.3	V
R_{thJC}				0.5	K/W

Features

- ISOPLUS247™ package with DCB Base
 - Electrical isolation towards the heatsink
 - Low coupling capacitance to the heatsink for reduced EMI
 - High power dissipation
 - High temperature cycling capability of chip on DCB
 - JEDEC TO-247AD compatible
 - Easy clip assembly
- fast CoolMOS™ 1) power MOSFET 3rd generation
 - High blocking capability
 - Low on resistance
 - Avalanche rated for unclamped inductive switching (UIS)
 - Low thermal resistance due to reduced chip thickness
- Enhanced total power density

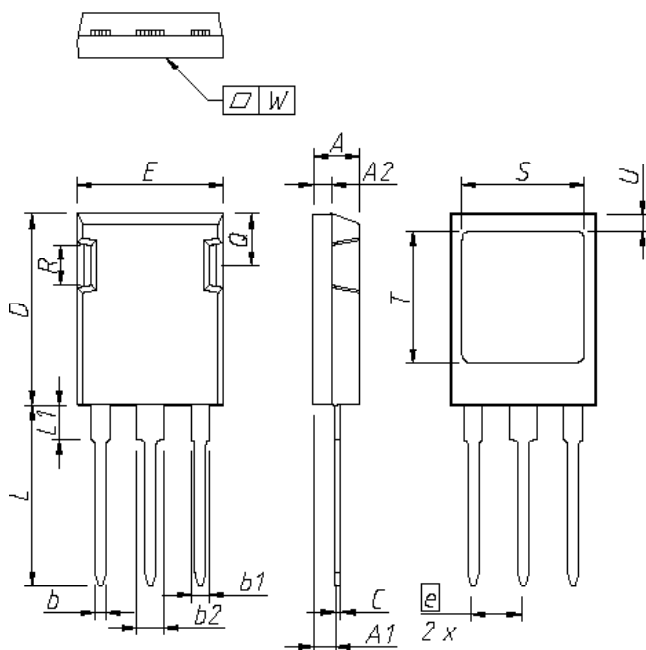
Applications

- Switched mode power supplies (SMPS)
- Uninterruptible power supplies (UPS)
- Power factor correction (PFC)
- Welding
- Inductive heating

1) CoolMOS™ is a trademark of Infineon Technologies AG.

Component			
Symbol	Conditions	Maximum Ratings	
V_{ISOL}	$I_{ISOL} \leq 1 \text{ mA}; 50/60 \text{ Hz}$	2500	V~
T_{VJ}		-40...+150	°C
T_{stg}		-40...+125	°C
T_L	1.6 mm from case for 10 s	300	°C
F_c	mounting force with clip	20 ... 120	N

Symbol	Conditions	Characteristic Values		
		min.	typ.	max.
C_p	coupling capacity bewtween shorted pin and mounting tab in the case		30	pF
R_{thCH}	with heatsink compound		0.25	K/W
Weight			6	g



DIM.	MILLIMETER		INCHES	
	MIN	MAX	MIN	MAX
A	4,83	5,21	0,190	0,205
A1	2,29	2,54	0,090	0,100
A2	1,91	2,16	0,075	0,085
b	1,14	1,40	0,045	0,055
b1	1,91	2,15	0,075	0,085
b2	2,92	3,20	0,115	0,126
C	0,61	0,83	0,024	0,033
D	20,80	21,34	0,819	0,840
E	15,75	16,13	0,620	0,635
e	5,45 BSC		0,215 BSC	
L	19,81	20,60	0,780	0,811
L1	3,81	4,38	0,150	0,172
Q	5,59	6,20	0,220	0,244
R	4,32	4,85	0,170	0,191
S	13,21	13,72	0,520	0,540
T	15,75	16,26	0,620	0,640
U	1,65	2,03	0,065	0,080
W	-	0,10	-	0,004

Die konvexe Form des Substrates ist typ. < 0.04 mm über der Kunststoffoberfläche der Bauteilunterseite
 The convex bow of substrate is typ. < 0.04 mm over plastic surface level of device bottom side

Die Gehäuseabmessungen entsprechen dem Typ TO-247 AD gemäß JEDEC außer Schraubloch und L_{max} .
 This drawing will meet all dimensions requirement of JEDEC outline TO-247 AD except screw hole and except L_{max} .



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