

High Voltage Power MOSFET

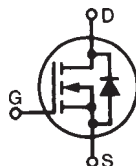
IXTH2N150

$$V_{DSS} = 1500V$$

$$I_{D25} = 2A$$

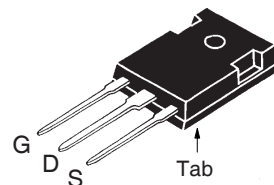
$$R_{DS(on)} \leq 9.2\Omega$$

N-Channel Enhancement Mode
Fast Intrinsic Diode



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	1500	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	1500	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ C$	2	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	6	A
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$	5	V/ns
P_D	$T_C = 25^\circ C$	170	W
T_J		- 55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		- 55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
M_d	Mounting Torque	1.13 / 10	Nm/lb.in
Weight		6	g

TO-247



G = Gate D = Drain
S = Source Tab = Drain

Features

- International Standard Package
- Fast Intrinsic Diode
- Molding Epoxies meet UL 94 V-0 Flammability Classification

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- High Voltage Power Supplies
- Capacitor Discharge Applications
- Pulse Circuits

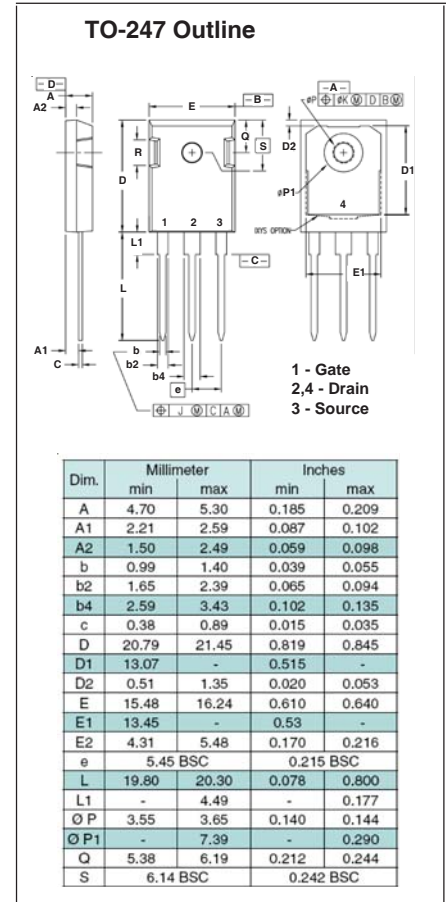
Symbol	Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu A$	1500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	2.5		5.0 V
I_{GSS}	$V_{GS} = \pm 30V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$			10 μA 400 μA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			9.2 Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 20\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	1.5	2.5	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		830	pF
C_{oss}			64	pF
C_{rss}			24	pF
R_{GI}	Gate Input Resistance		5.1	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 10\Omega$ (External)		16	ns
t_r			26	ns
$t_{d(off)}$			55	ns
t_f			70	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$		28	nC
Q_{gs}			4	nC
Q_{gd}			16	nC
R_{thJC}			0.73	$^\circ\text{C/W}$
R_{thCS}		0.21		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$, Note 1			2 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			8 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			1.3 V
t_{rr}	$I_F = 1\text{A}$, $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}$		377	ns
Q_{RM}			1.7	μC
I_{RM}			9.2	A

Note: 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.



ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

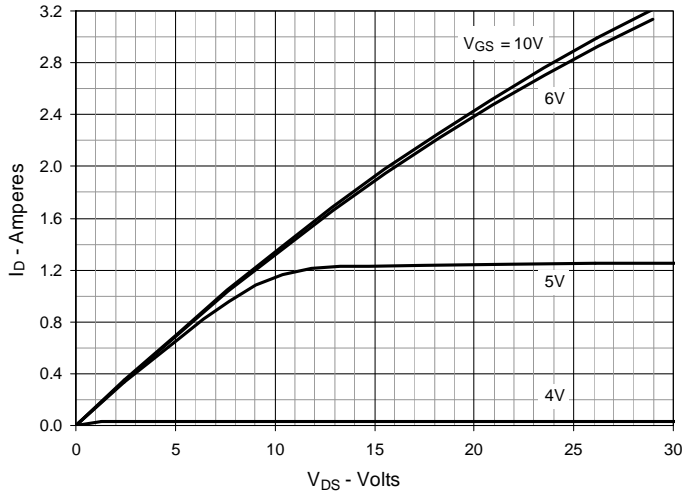
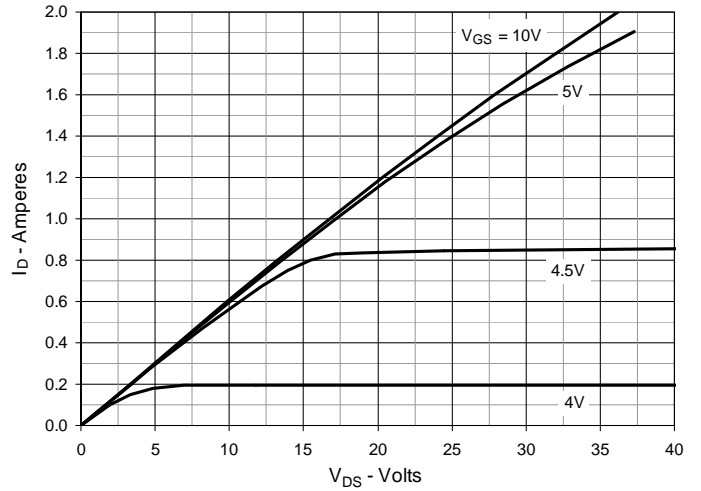
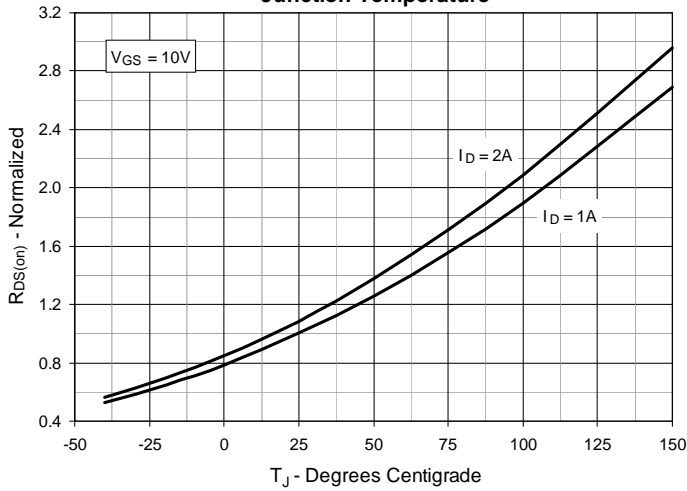
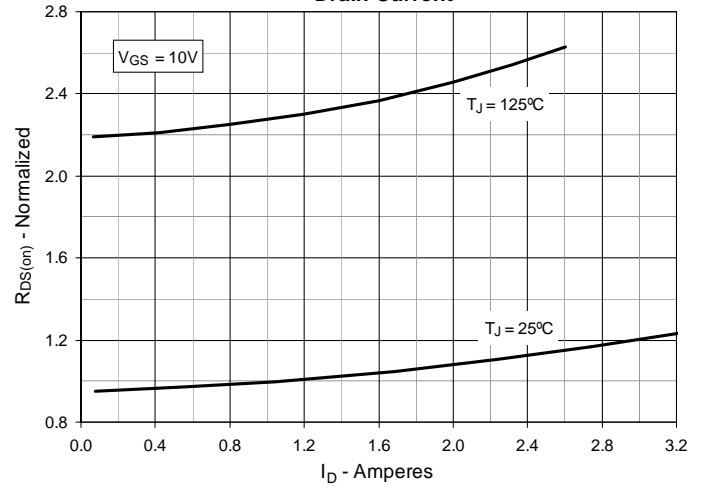
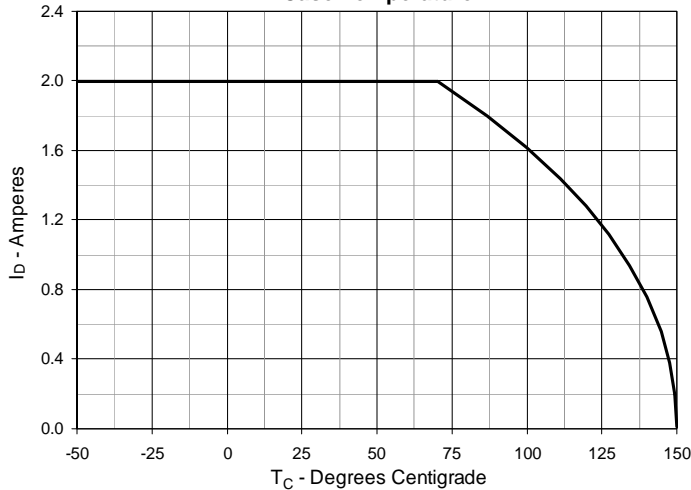
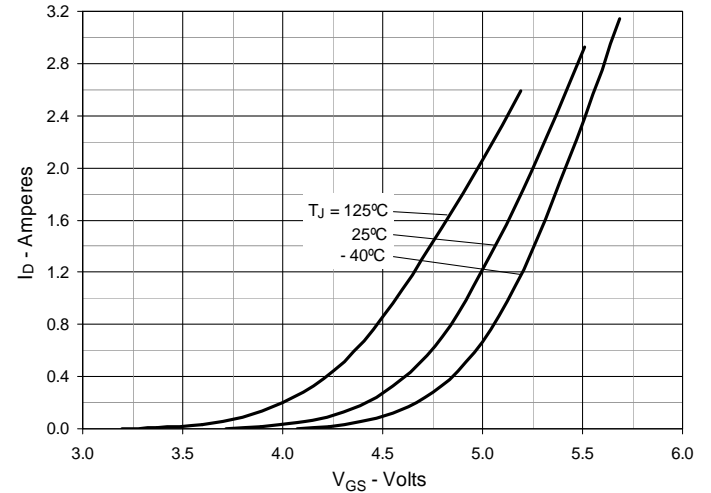
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 3. $R_{DS(on)}$ Normalized to $I_D = 1\text{A}$ Value vs. Junction Temperature

Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 1\text{A}$ Value vs. Drain Current

Fig. 5. Maximum Drain Current vs. Case Temperature

Fig. 6. Input Admittance


Fig. 7. Transconductance

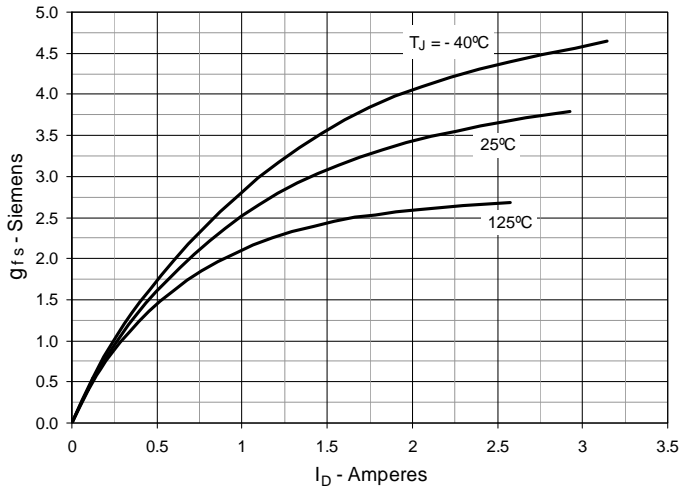


Fig. 8. Forward Voltage Drop of Intrinsic Diode

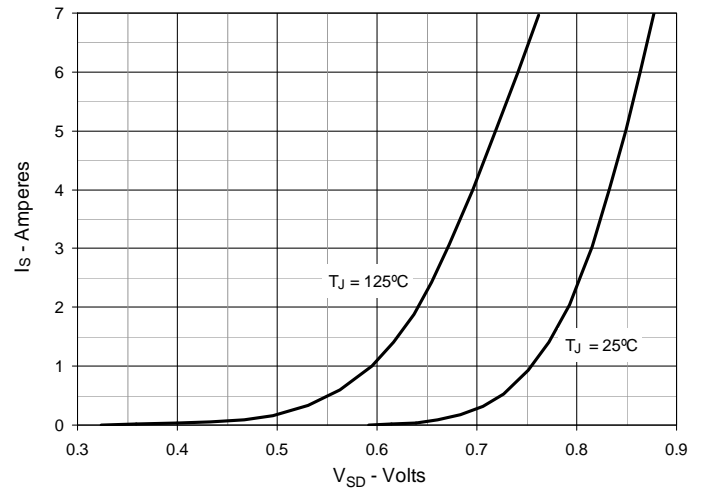


Fig. 9. Gate Charge

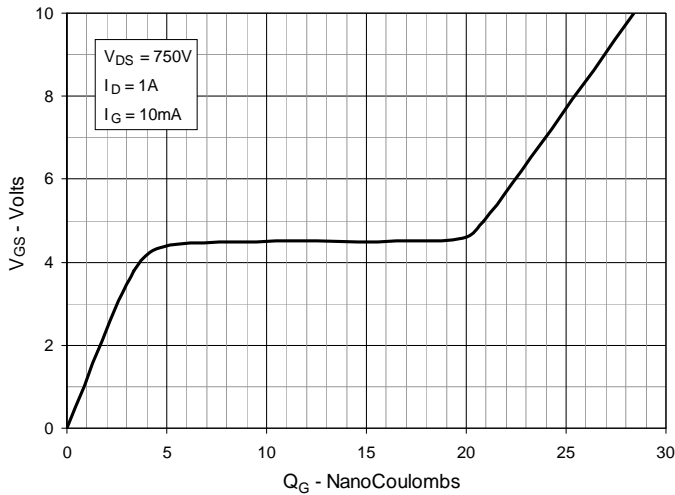


Fig. 10. Capacitance

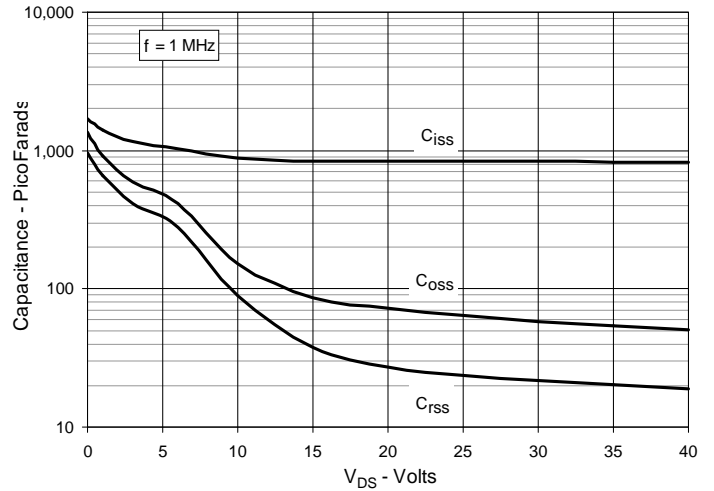


Fig. 11. Forward-Bias Safe Operating Area

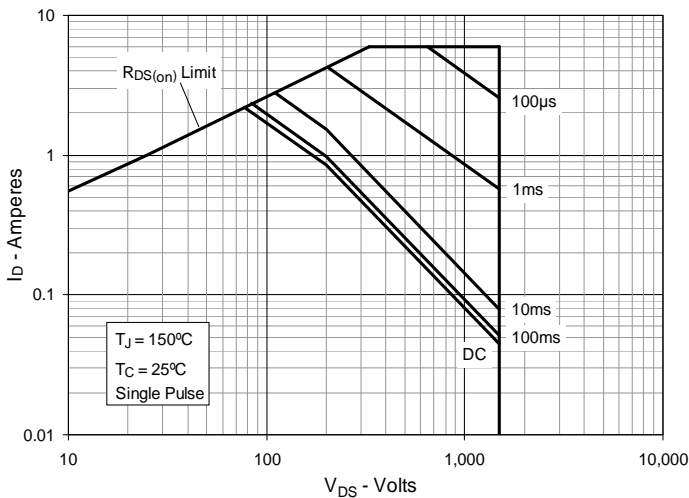
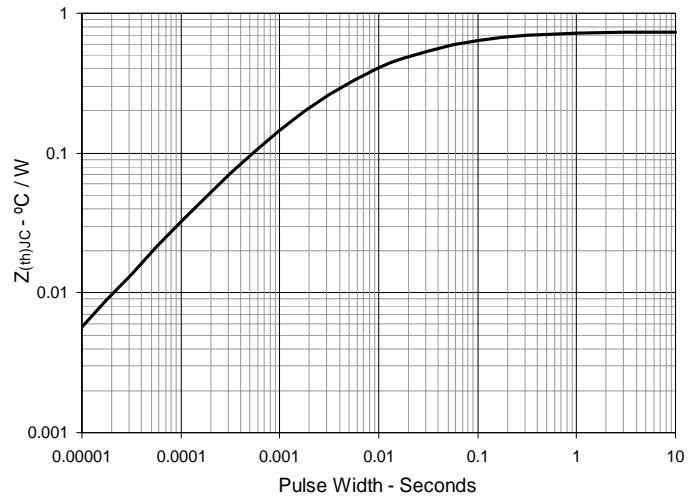


Fig. 12. Maximum Transient Thermal Impedance





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