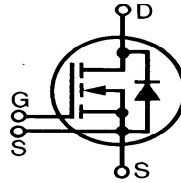


Q3-Class HiperFET™ Power MOSFET

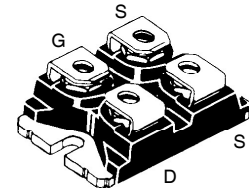
IXFN100N50Q3

$V_{DSS} = 500V$
 $I_{D25} = 82A$
 $R_{DS(on)} \leq 49m\Omega$
 $t_{rr} \leq 250ns$

N-Channel Enhancement Mode
Fast Intrinsic Rectifier



miniBLOC
E153432



G = Gate D = Drain
S = Source

Either Source Terminal S can be used as the Source Terminal or the Kelvin Source (Gate Return) Terminal.

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	500	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	500	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ C$	82	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	300	A
I_A	$T_C = 25^\circ C$	100	A
E_{AS}	$T_C = 25^\circ C$	5	J
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$	50	V/ns
P_D	$T_C = 25^\circ C$	960	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
V_{ISOL}	50/60 Hz, RMS, $t = 1$ minute	2500	V~
	$I_{ISOL} \leq 1mA$, $t = 1s$	3000	V~
M_d	Mounting Torque for Base Plate	1.5/13	Nm/lb.in.
	Terminal Connection Torque	1.3/11.5	Nm/lb.in.
Weight		30	g

Features

- International Standard Package
- Low Intrinsic Gate Resistance
- miniBLOC with Aluminum Nitride Isolation
- Low Package Inductance
- Fast Intrinsic Rectifier
- Low $R_{DS(on)}$ and Q_G

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- DC-DC Converters
- Battery Chargers
- Switch-Mode and Resonant-Mode Power Supplies
- DC Choppers
- Temperature and Lighting Controls

Symbol	Test Conditions ($T_J = 25^\circ C$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 3mA$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8mA$	3.5		6.5 V
I_{GSS}	$V_{GS} = \pm 30V$, $V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$			50 μA 2.5 mA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 50A$, Note 1			49 m Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 20\text{V}, I_D = 50\text{A}$, Note 1	40	65	S
C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		13.8	nF
C_{oss}			1690	pF
C_{rss}			177	pF
R_{Gi}	Gate Input Resistance		0.12	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 50\text{A}$ $R_G = 0.5\Omega$ (External)		40	ns
t_r			20	ns
$t_{d(off)}$			50	ns
t_f			15	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 50\text{A}$		255	nC
Q_{gs}			110	nC
Q_{gd}			115	nC
R_{thJC}				0.13 $^\circ\text{C/W}$
R_{thCS}		0.05		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			100 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			400 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{V}$, Note 1			1.5 V
t_{rr}	$I_F = 50\text{A}, -di/dt = 200\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GS} = 0\text{V}$			250 ns
Q_{RM}			3.5	μC
I_{RM}			30.0	A

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
by one or more of the following U.S. patents:	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

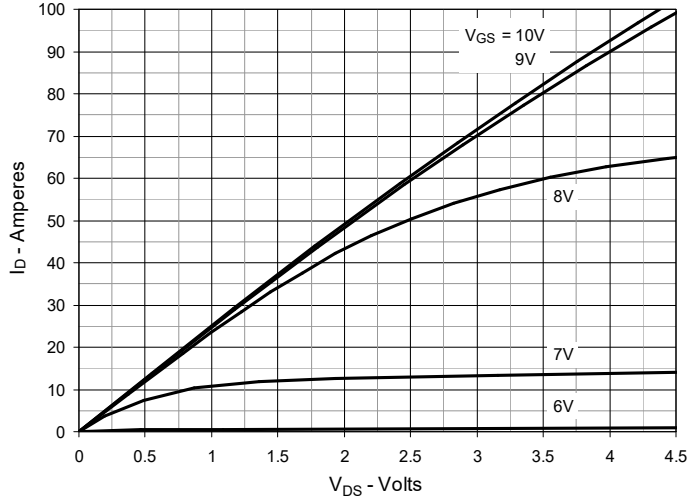


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

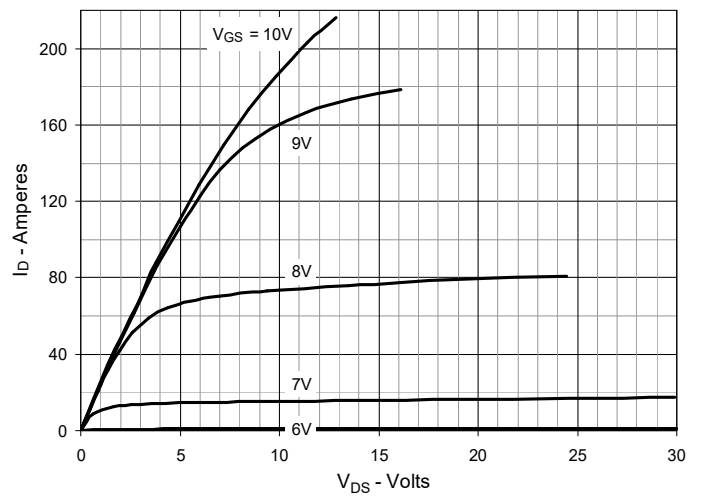


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

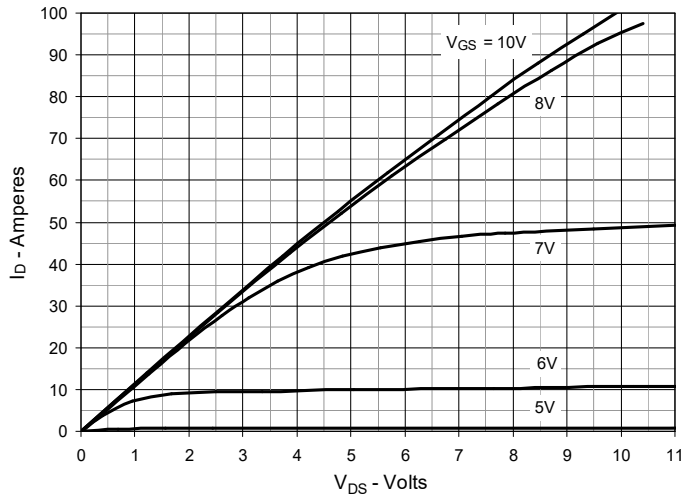


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 50A$ Value vs. Junction Temperature

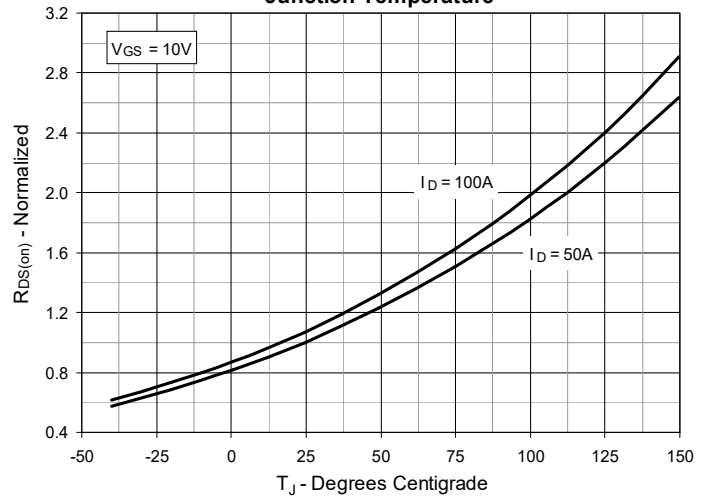


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 50A$ Value vs. Drain Current

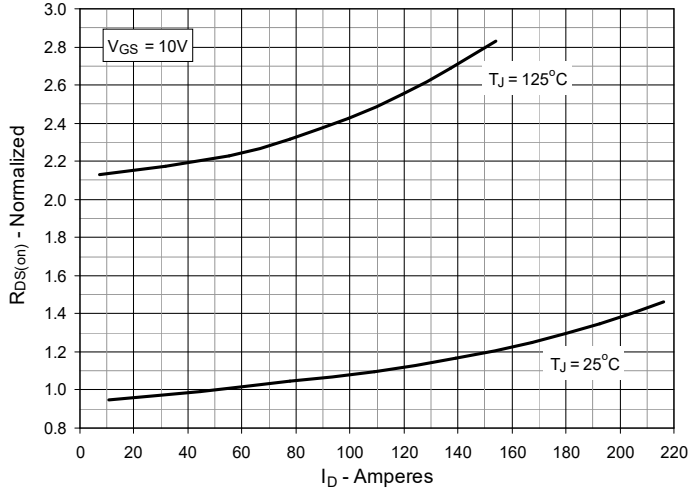


Fig. 6. Maximum Drain Current vs. Case Temperature

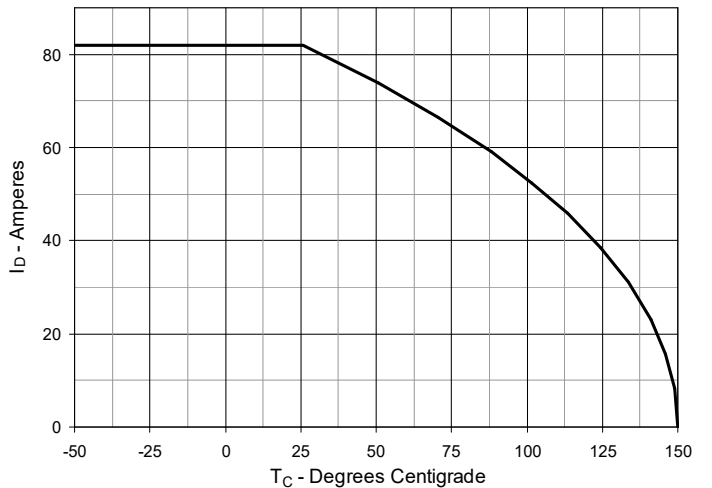


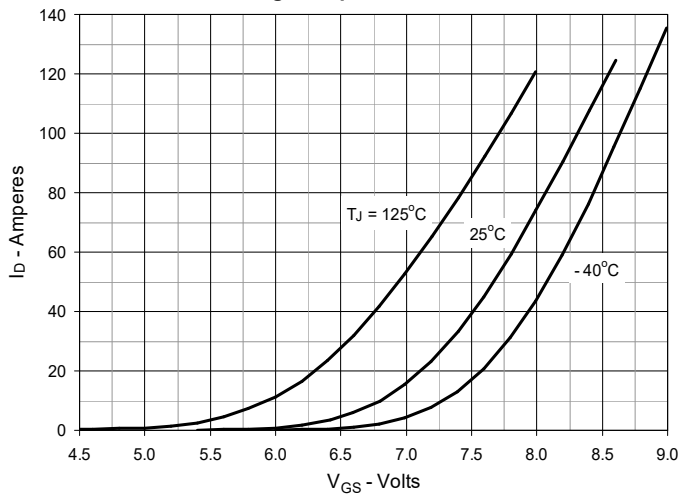
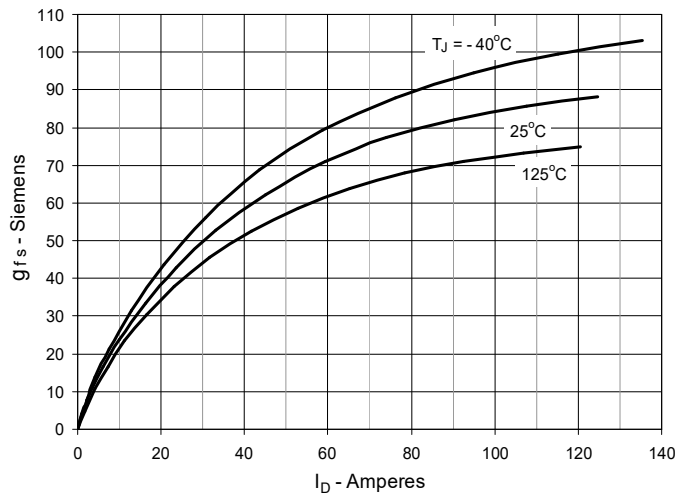
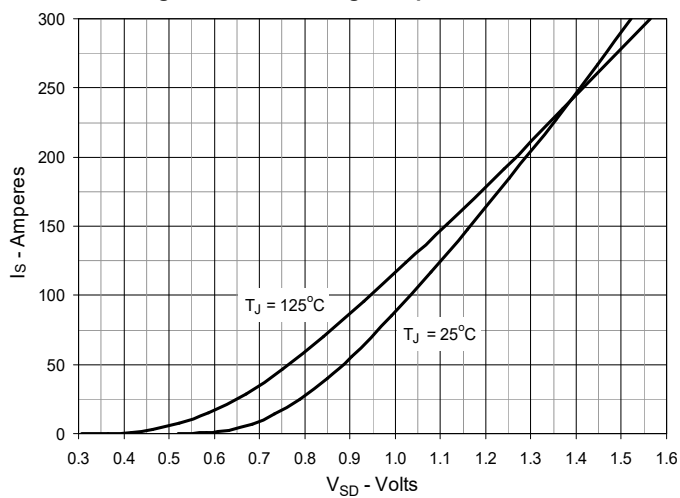
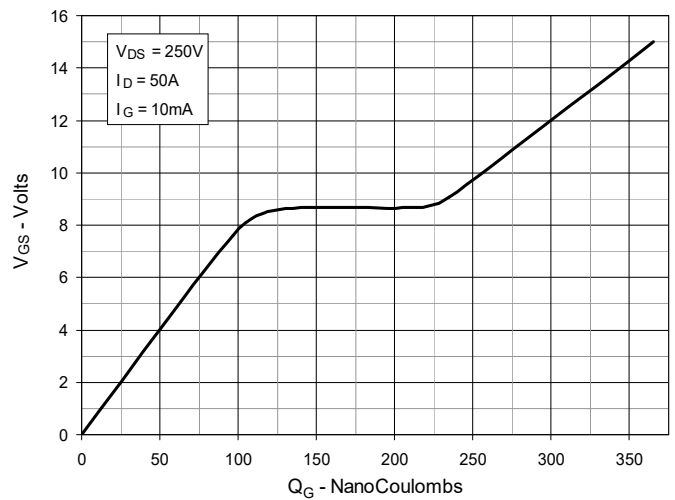
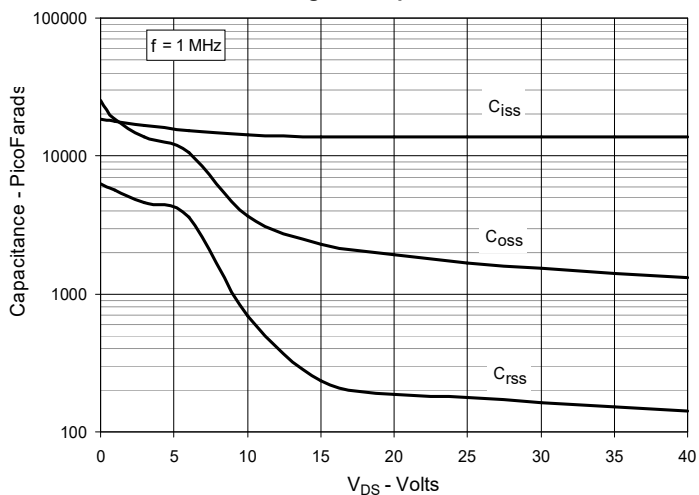
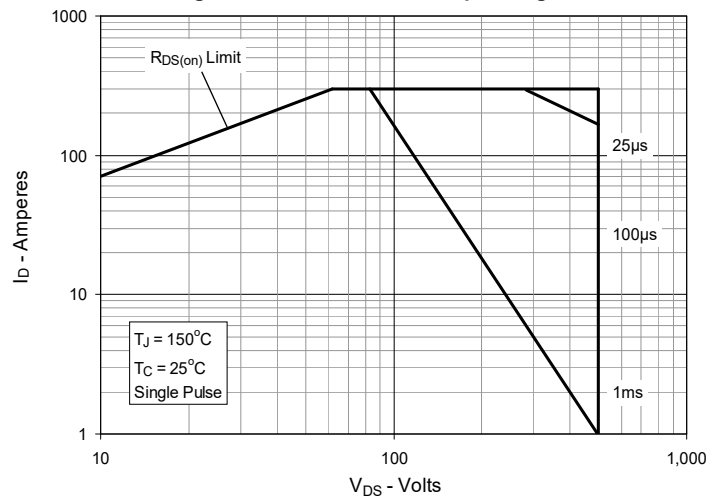
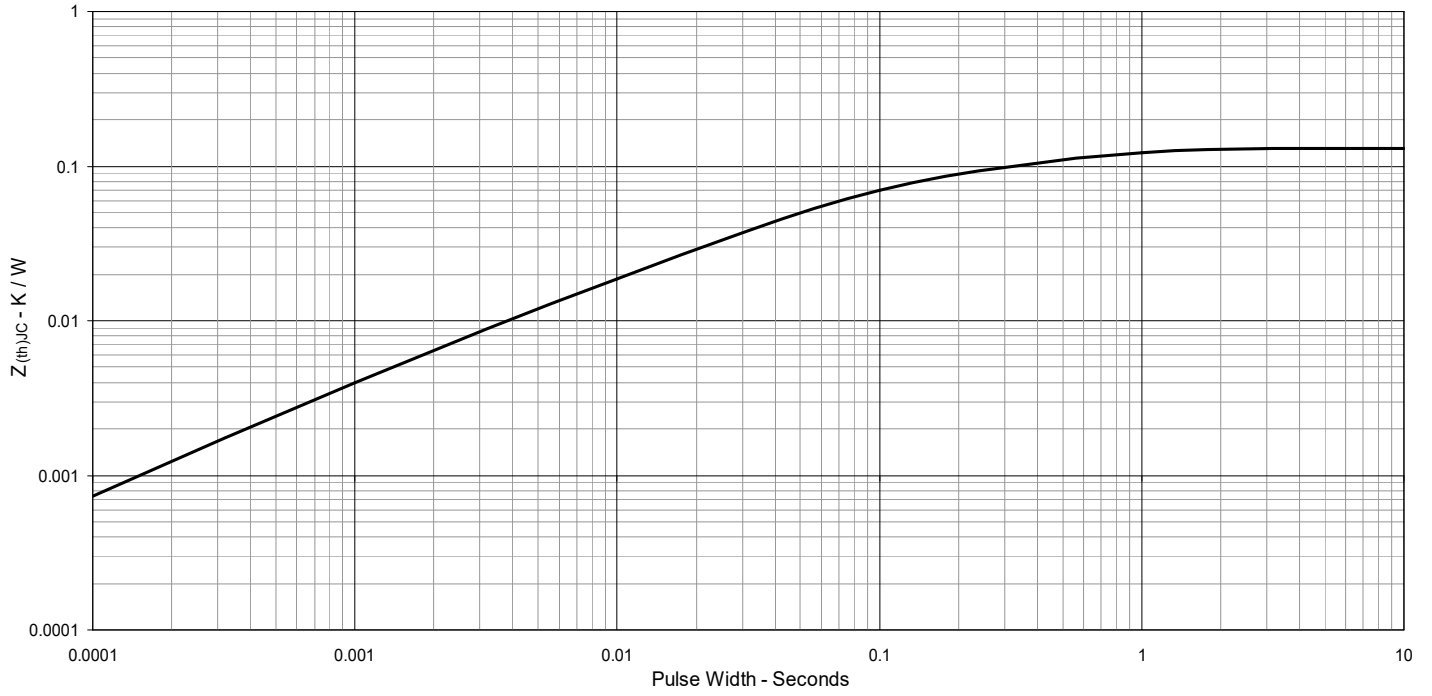
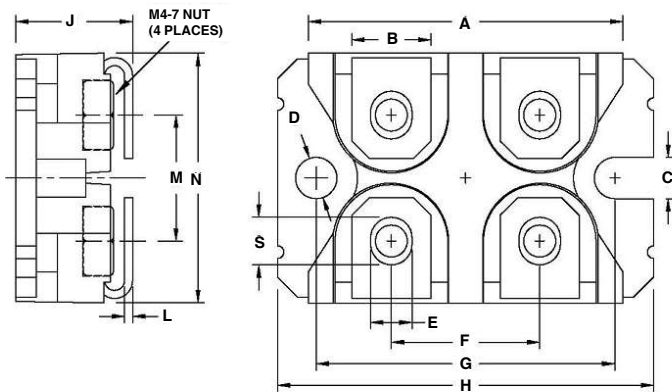
Fig. 7. Input Admittance

Fig. 8. Transconductance

Fig. 9. Forward Voltage Drop of Intrinsic Diode

Fig. 10. Gate Charge

Fig. 11. Capacitance

Fig. 12. Forward-Bias Safe Operating Area


Fig. 13. Maximum Transient Thermal Impedance



SOT-227 Outline


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.224	1.260	31.10	32.00
B	.303	.327	7.70	8.30
C	.161	.173	4.10	4.40
D	.161	.173	4.10	4.40
E	.161	.173	4.10	4.40
F	.587	.598	14.90	15.20
G	1.181	1.201	30.00	30.50
H	1.488	1.508	37.80	38.30
J	.461	.484	11.70	12.30
L	.030	.033	0.75	0.85
M	.492	.512	12.50	13.00
N	.984	1.004	25.00	25.50
O	.075	.087	1.90	2.20
S	.181	.193	4.60	4.90
U	.000	.005	0.00	0.13

- NUT MATERIAL:
 STANDARD - Low carbon steel with Ni plating.
 OPTIONAL: - Brass Nut is available.
 PART NUMBER-BN
- ALL METAL SURFACE ARE PRE NI PLATED EXCEPT TRIM AREA.



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