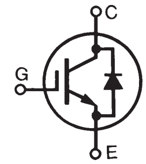
IXYS

GenX3™ 600V IGBT with Diode

IXGR48N60C3D1

V_{CES} = 600V
I_{C25} = 56A
$V_{CE(sat)}$ ≤ 2.7V
$t_{fi(typ)}$ = 38ns

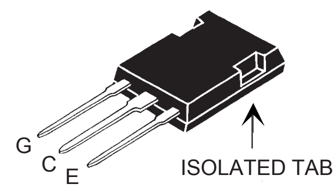
(Electrically Isolated Back Surface)



High Speed PT IGBTs for
40-100kHz Switching

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	600	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	600	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	56	A
I_{C110}	T_C = 110°C	26	A
I_{D110}	T_C = 110°C	27	A
I_{CM}	T_C = 25°C, 1ms	230	A
I_A	T_C = 25°C	30	A
E_{AS}	T_C = 25°C	300	mJ
SSOA	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 3Ω	I_{CM} = 100	A
(RBSOA)	Clamped Inductive Load	@ V_{CE} ≤ 600	V
P_C	T_C = 25°C	125	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10 Seconds	260	°C
V_{ISOL}	50/60 Hz RMS, t = 1min	2500	V~
F_C	Mounting Force	20..120 / 4.5..27	N/lb.
Weight		5	g

ISOPLUS 247™



G = Gate C = Collector
E = Emitter

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
  - UL Recognized Package
  - Isolated Mounting Surface
  - 2500V Electrical Isolation
- Avalanche Rated
- Square RBSOA
- Anti-Parallel Ultra Fast Diode
- Fast Switching
- International Standard Package

Advantages

- High Power Density
- Low Gate Drive Requirement

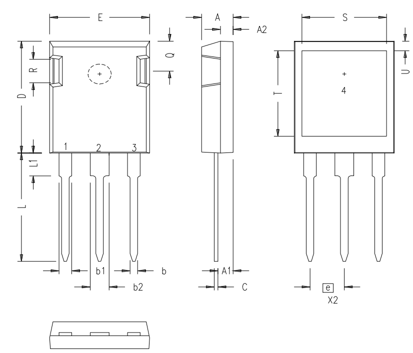
Applications

- High Frequency Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, Unless Otherwise Specified) Min.	Typ.	Max.	
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}		3.0		5.5	V
I_{CES}	V_{CE} = V_{CES}				300	μA
	V_{GE} = 0V	T_J = 125°C			1.75	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V				±100	nA
$V_{CE(sat)}$	I_C = 30A, V_{GE} = 15V, Note 1			2.3	2.7	V
		T_J = 125°C		1.8		V

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Min.	Typ.	Max.	
g_{fs}	I_C = 30A V_{CE} = 10V, Note 1	20	30		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		1960		pF
C_{oes}			220		pF
C_{res}			66		pF
Q_g	I_C = 30A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		77		nC
Q_{ge}			16		nC
Q_{gc}			32		nC
$t_{d(on)}$	**Inductive Load, T_J = 25°C**		19		ns
t_{ri}	I_C = 30A, V_{GE} = 15V		26		ns
E_{on}	V_{CE} = 400V, R_G = 3Ω		0.41		mJ
$t_{d(off)}$			60	100	ns
t_{fi}			38		ns
E_{off}			0.23	0.55	mJ
$t_{d(on)}$	**Inductive Load, T_J = 125°C**		19		ns
t_{ri}	I_C = 30A, V_{GE} = 15V		26		ns
E_{on}	V_{CE} = 400V, R_G = 3Ω		0.65		mJ
$t_{d(off)}$			92		ns
t_{fi}			95		ns
E_{off}			0.57		mJ
R_{thJC}				1.0	°C/W
R_{thCS}			0.15		°C/W

ISOPLUS247 (IXGR) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Reverse Diode (FRED)

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)		Min.	Typ.	Max.	
V_F	I_F = 30A, V_{GE} = 0V, Note 1	T_J =25°C			2.7	V
I_{RM}	I_F = 30A, V_{GE} = 0V, $-di_F/dt$ =100A/µs,	T_J = 100°C			4	A
t_{rr}	V_R = 100V	T_J =100°C		100		ns
	I_F = 1A, -di/dt = 100A/µs; V_R = 30V			25		ns
R_{thJC}					1.5	°C/W

Note 1: Pulse test, t ≤ 300µs, Duty cycle, d ≤ 2 %.

Fig. 1. Output Characteristics @ 25ºC

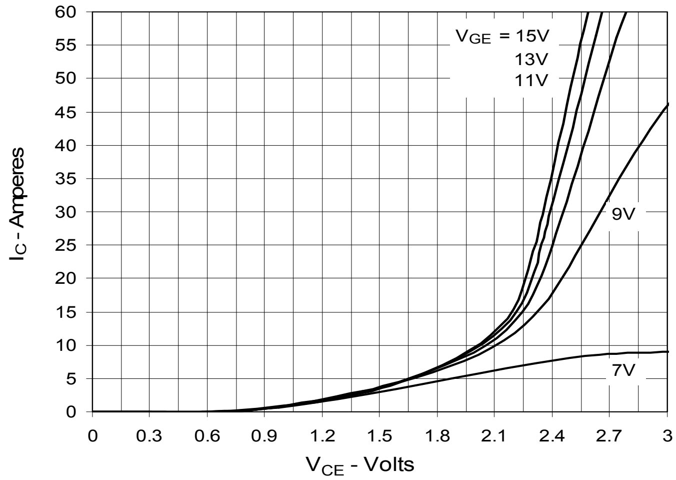


Fig. 2. Extended Output Characteristics @ 25ºC

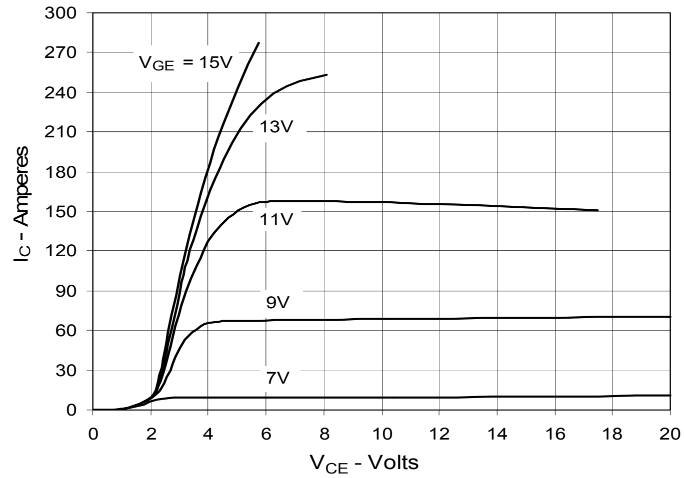


Fig. 3. Output Characteristics @ 125ºC

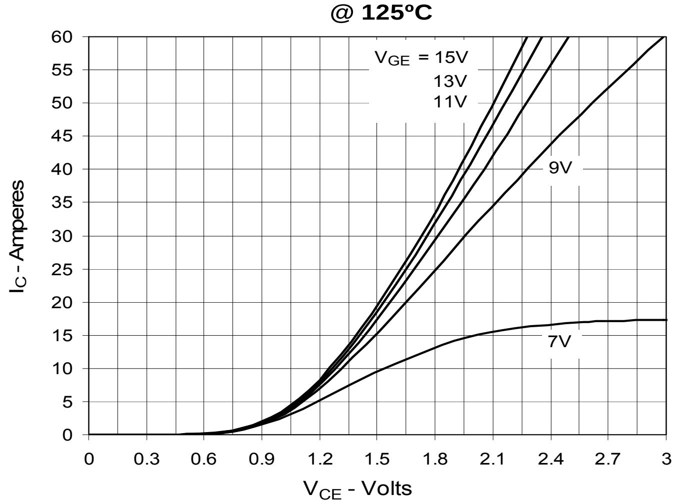


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

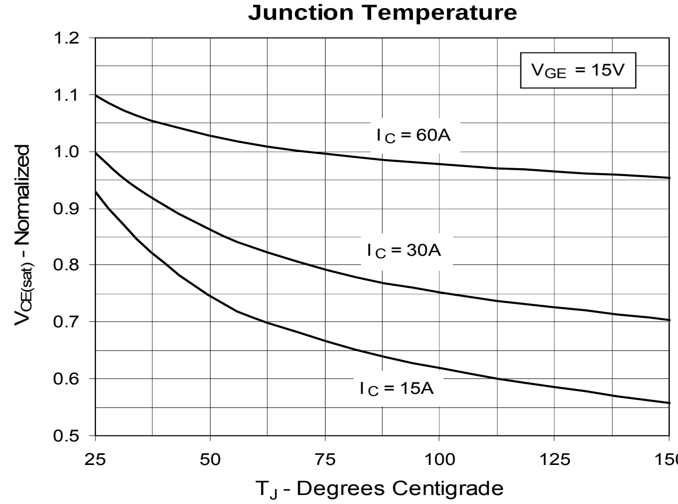


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

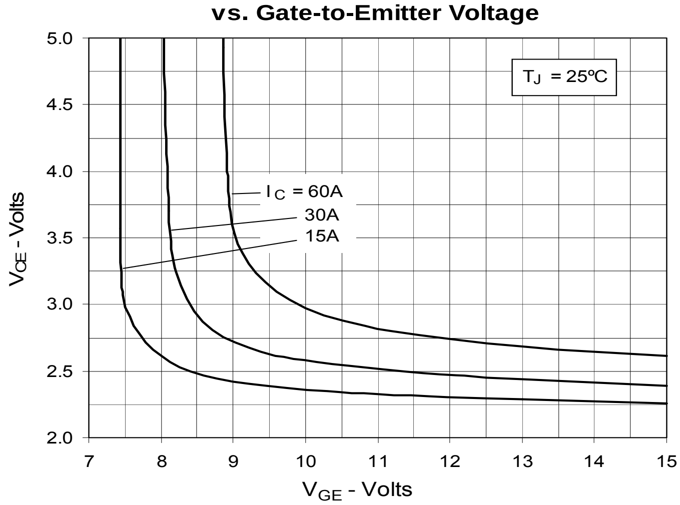


Fig. 6. Input Admittance

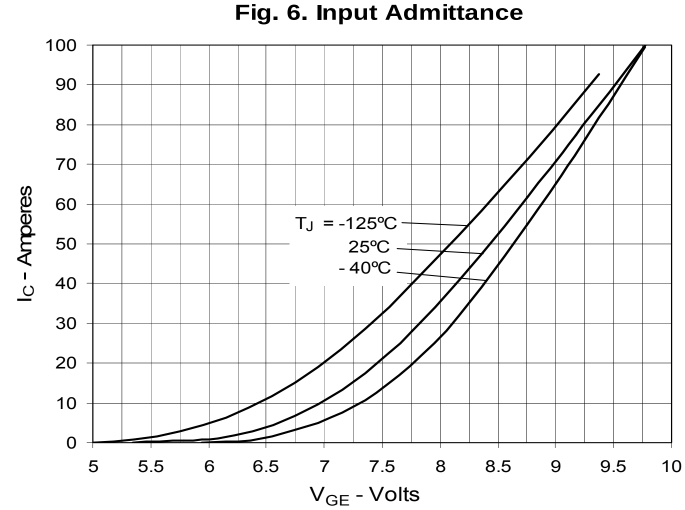


Fig. 7. Transconductance

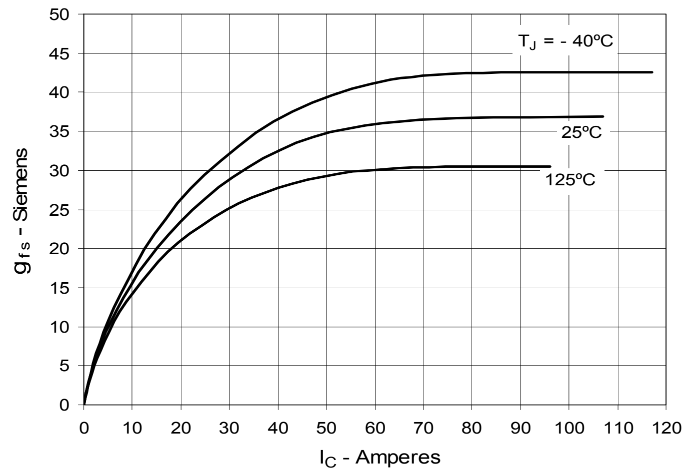


Fig. 8. Gate Charge

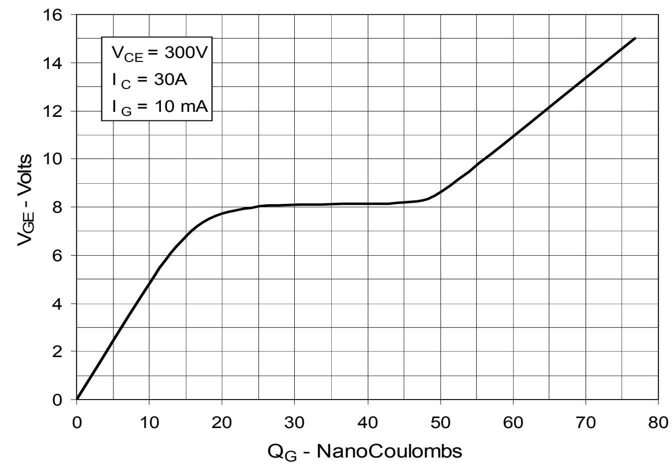


Fig. 9. Capacitance

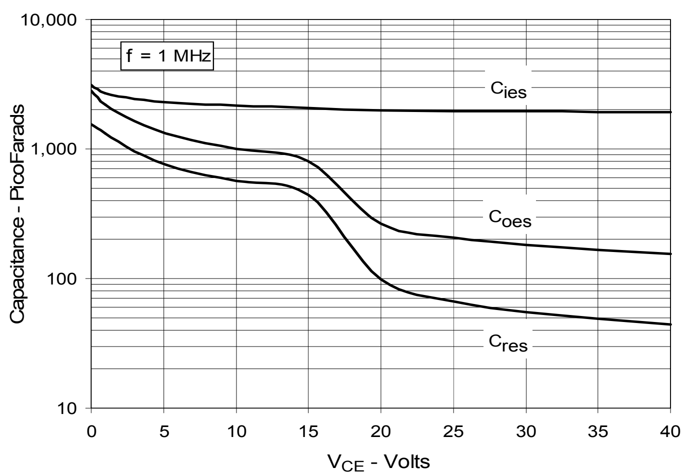


Fig. 10. Reverse-Bias Safe Operating Area

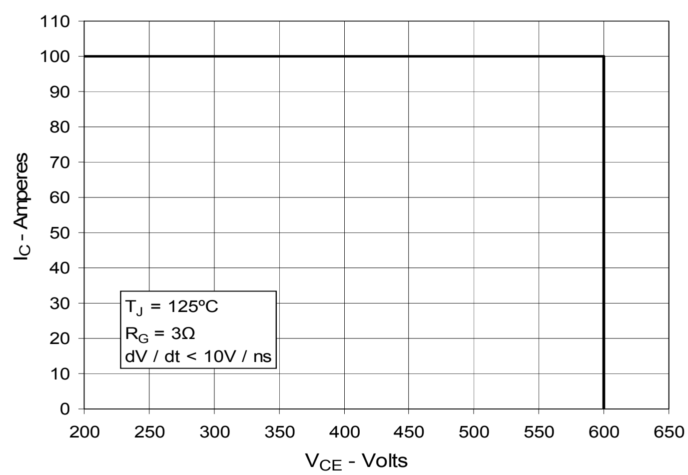
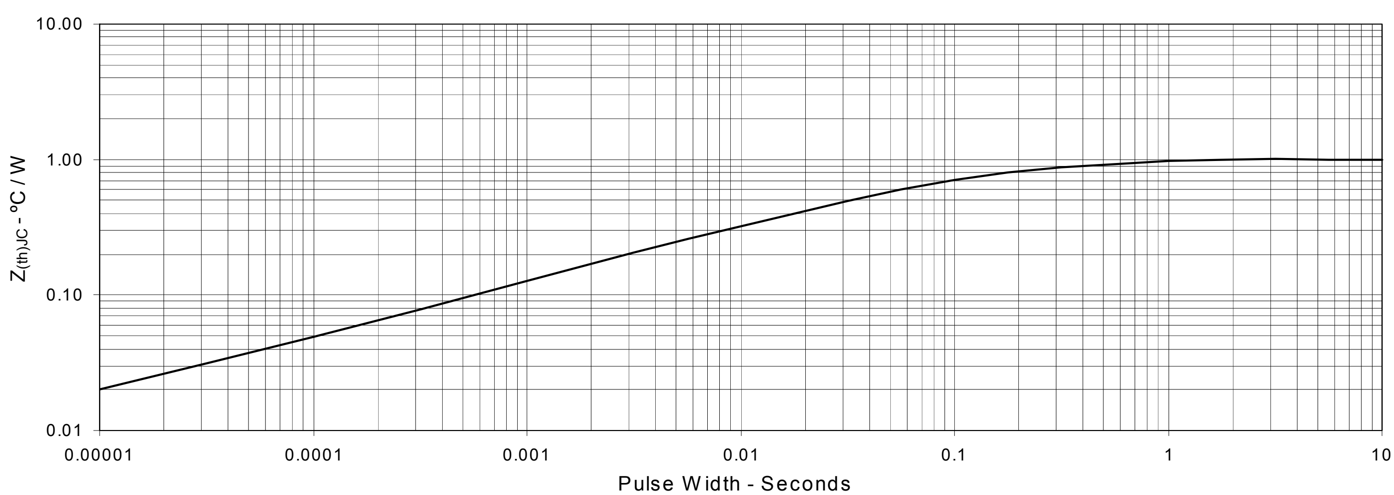


Fig. 11. Maximum Transient Thermal Impedance



IXYS reserves the right to change limits, test conditions, and dimensions.

Fig. 12. Inductive Switching Energy Loss vs. Gate Resistance

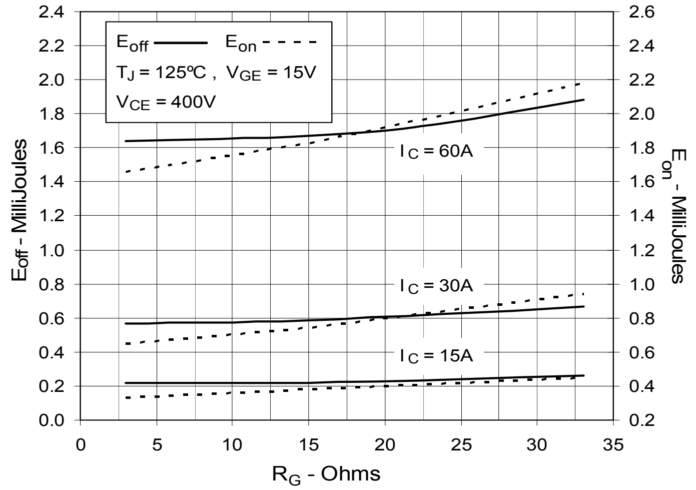


Fig. 13. Inductive Swiching Energy Loss vs. Collector Current

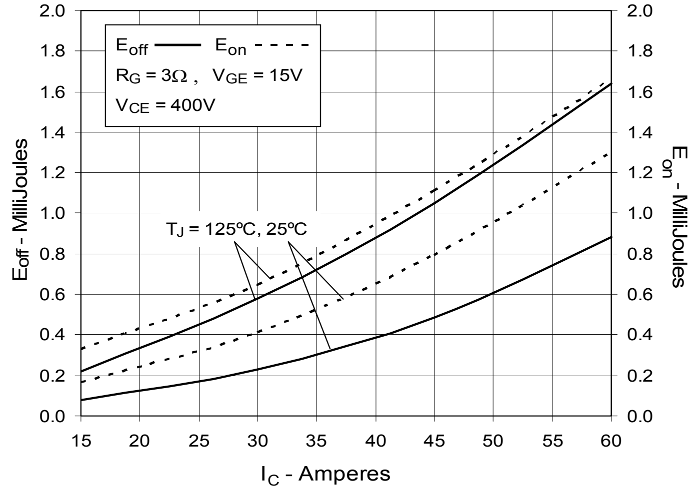


Fig. 14. Inductive Swiching Energy Loss vs. Junction Temperature

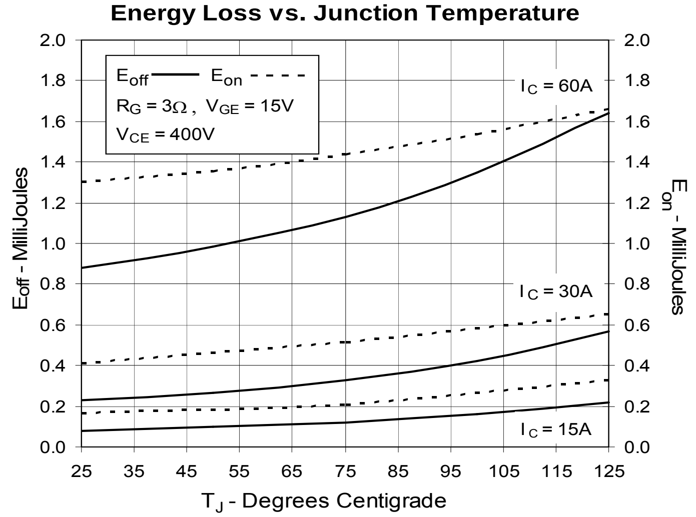


Fig. 15. Inductive Turn-off Switching Times vs. Gate Resistance

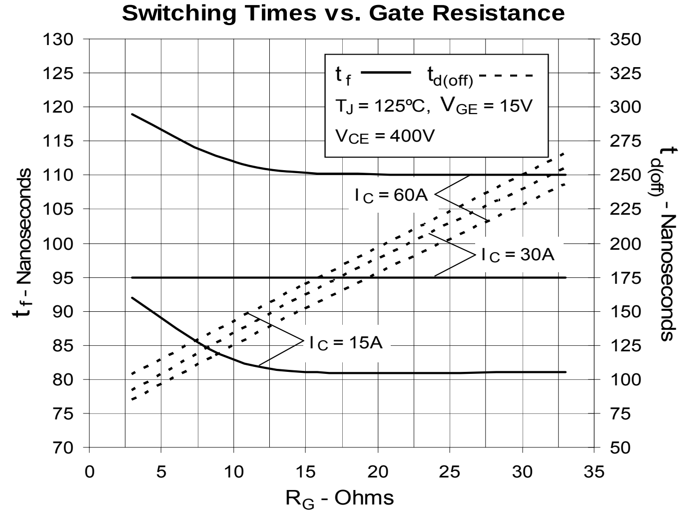


Fig. 16. Inductive Turn-off Switching Times vs. Collector Current

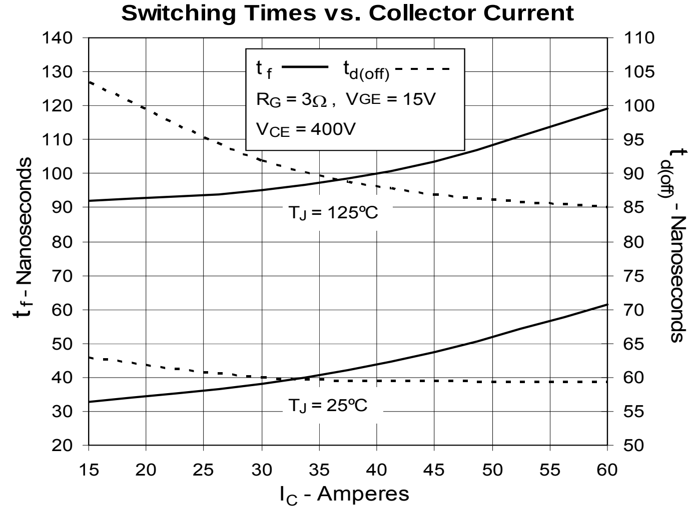


Fig. 17. Inductive Turn-off Switching Times vs. Junction Temperature

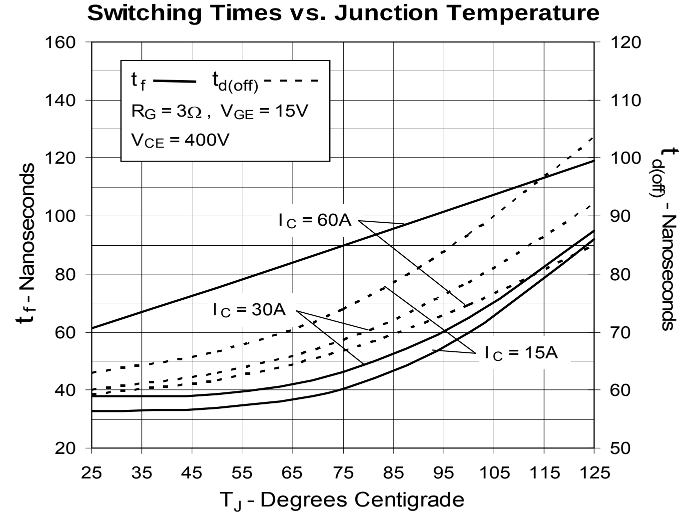


Fig. 18. Inductive Turn-on Switching Times vs. Gate Resistance

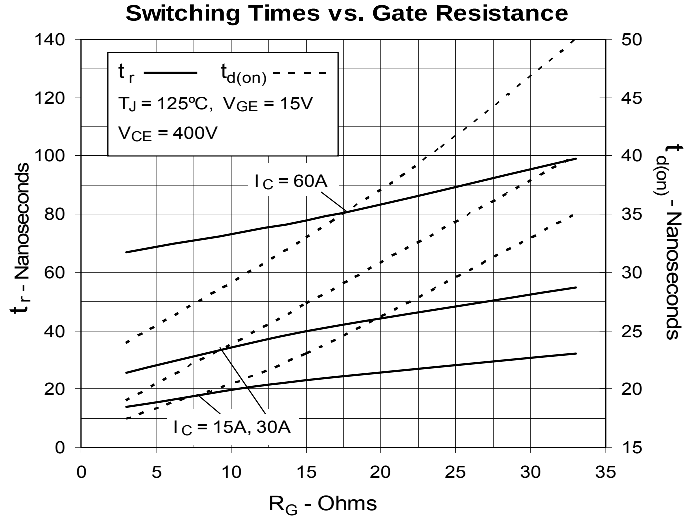


Fig. 19. Inductive Turn-on Switching Times vs. Collector Current

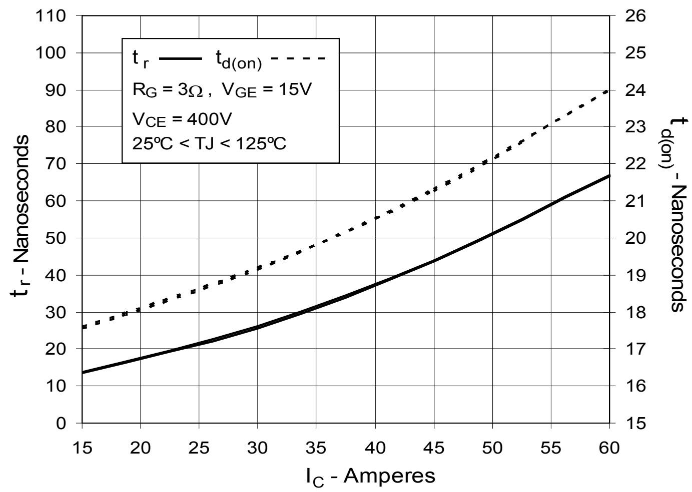
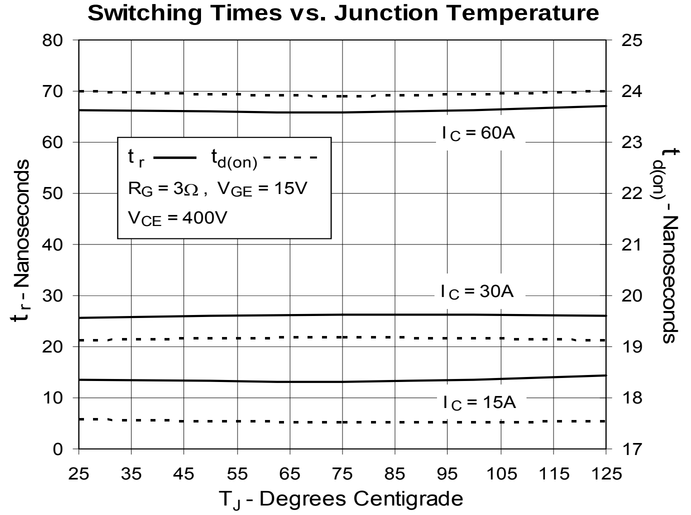


Fig. 20. Inductive Turn-on Switching Times vs. Junction Temperature



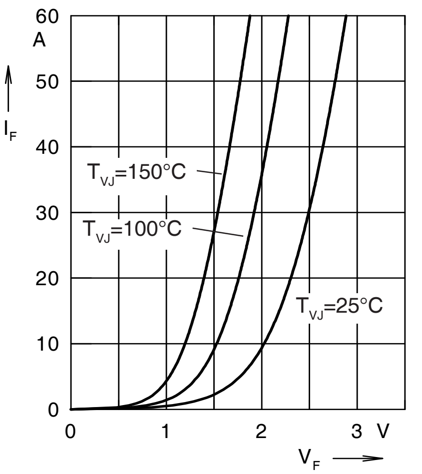


Fig. 21. Forward current I_F versus V_F

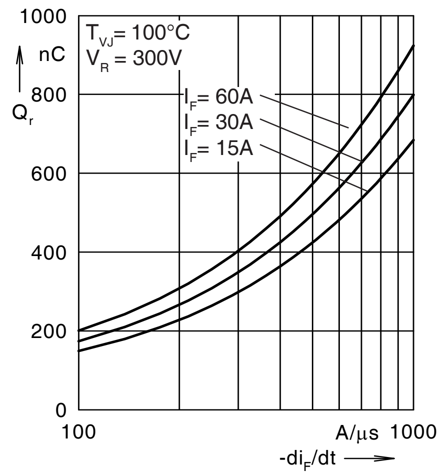


Fig. 22. Reverse recovery charge Q_r versus $-di_F/dt$

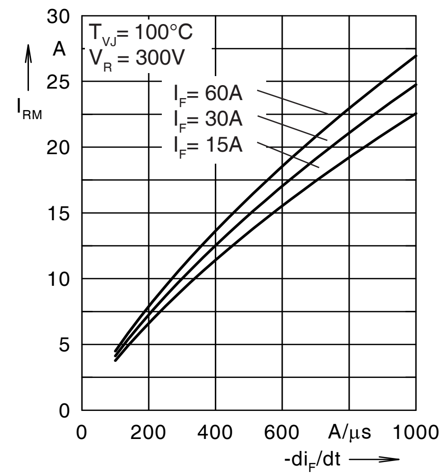


Fig. 23. Peak reverse current I_{RM} versus $-di_F/dt$

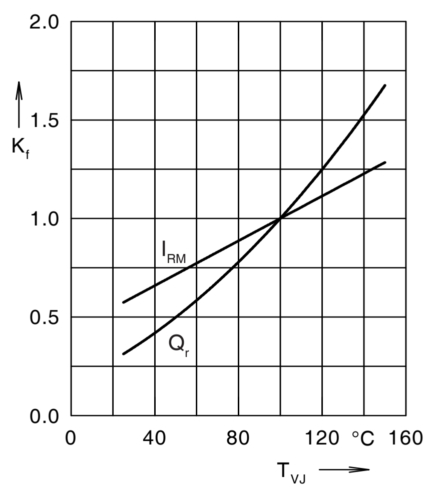


Fig. 24. Dynamic parameters Q_r, I_{RM} versus T_{VJ}

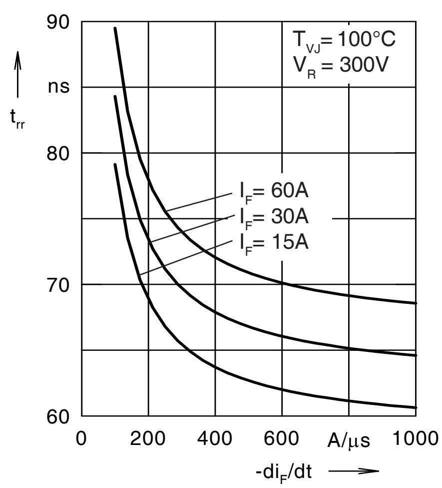


Fig. 25. Recovery time t_{rr} versus $-di_F/dt$

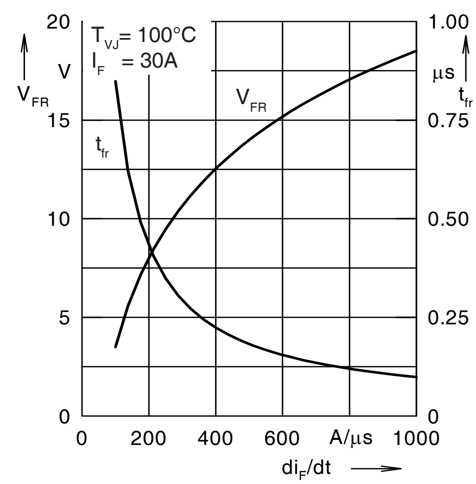


Fig. 26. Peak forward voltage V_{FR} and t_{fr} versus di_F/dt

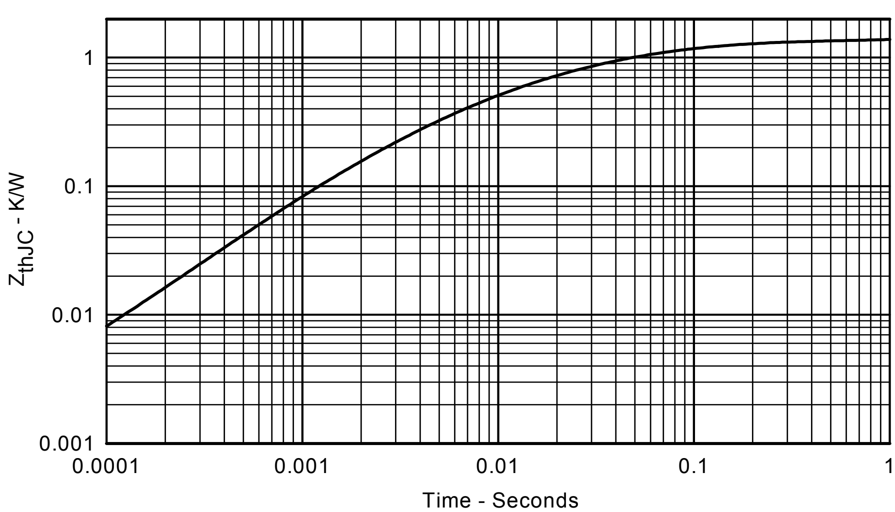


Fig. 27. Transient thermal resistance junction to case