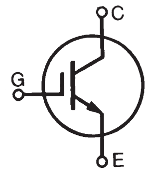
IXYS

Very High Voltage IGBT

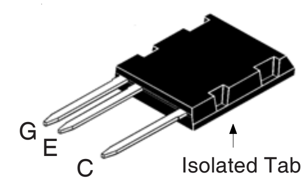
IXEL40N400

V_{CES} = 4000V
I_{C110} = 40A
$V_{CE(sat)}$ ≤ 3.2V
$t_{fi(typ)}$ = 425ns

(Electrically Isolated Tab)



ISOPLUS i5-Pak™



G = Gate C = Collector
E = Emitter

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	4000	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	90	A
I_{C110}	T_C = 110°C	40	A
I_{CM}	Pulse Width Limited by T_{JM}, 1ms, V_{GE} = 25V	400	A
P_C	T_C = 25°C	380	W
T_J		- 40 ... +150	°C
T_{JM}		150	°C
T_{stg}		- 40 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10s	260	°C
V_{ISOL}	I_{ISOL} < 1mA, 50/60 Hz, t = 1 minute	4000	V~
F_C	Mounting Force	30..170 / 7..36	Nm/lb-in.
Weight		8	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
$V_{GE(th)}$	I_C = 10mA, V_{CE} = V_{GE}	5.5		7.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			100	μA
	Note 2, T_J = 125°C		1.5		mA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±500	nA
$V_{CE(sat)}$	I_C = I_{C110}, V_{GE} = 15V, Note 1		2.4	3.2	V
	T_J = 125°C		3.0		V

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- UL Recognized Package
- High Peak Current Capability
- Low Saturation Voltage
- Molding Epoxies Meet UL 94 V-0 Flammability Classification

Advantages

- High Power Density
- Easy to Mount

Applications

- Capacitor Discharge
- Pulser Circuits

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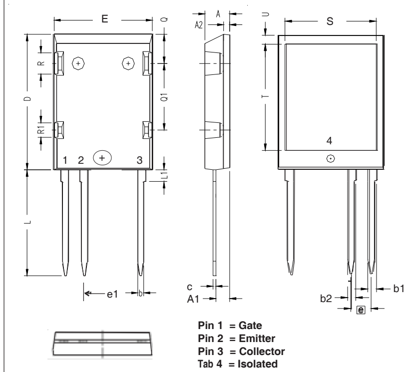
Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	$I_C = I_{C110}$, V_{CE} = 10V, Note 1	14	24	S
I_{SC}	$I_C = I_{C110}$, V_{CC} = 3400V, V_{CM} < 4000V; V_{GE} = 15V, $t_{SC} \leq$ 10µs		200	A
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		6040	pF
C_{oes}			278	pF
C_{res}			120	pF
R_{Gint}			5.2	Ω
$Q_{g(on)}$	$I_C = I_{C110}$, V_{GE} = 15V, V_{CE} = 1000 V		275	nC
Q_{ge}			63	nC
Q_{gc}			134	nC
$t_{d(on)}$	**Inductive load, T_J = 25°C**		160	ns
t_{ri}	$I_C = I_{C110}$, V_{GE} = 15V		100	ns
E_{on}	V_{CE} = 2800V, R_G = 33Ω		55	mJ
$t_{d(off)}$	Note 3		630	ns
t_{fi}			425	ns
E_{off}			165	mJ
$t_{d(on)}$	**Inductive load, T_J = 125°C**		155	ns
t_{ri}	$I_C = I_{C110}$, V_{GE} = 15V		105	ns
E_{on}	V_{CE} = 2800V, R_G = 33Ω		85	mJ
$t_{d(off)}$	Note 3		715	ns
t_{fi}			455	ns
E_{off}			205	mJ
R_{thJC}				0.26 °C/W
R_{thCK}	(Pressure Mount)		0.15	°C/W

ISOPLUS i5-Pak™ HV Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.190	0.205	4.83	5.21
A1	0.102	0.118	2.59	3.00
A2	0.046	0.055	1.17	1.40
b	0.045	0.055	1.14	1.40
b1	0.063	0.072	1.60	1.83
b2	0.058	0.068	1.47	1.73
c	0.020	0.029	0.51	0.74
D	1.020	1.040	25.91	26.42
E	0.770	0.799	19.56	20.29
e	0.150 BSC		3.81 BSC	
e1	0.450 BSC		11.43 BSC	
L	0.780	0.820	19.81	20.83
L1	0.080	0.102	2.03	2.59
Q	0.210	0.235	5.33	5.97
Q1	0.490	0.513	12.45	13.03
R	0.150	0.180	3.81	4.57
R1	0.100	0.130	2.54	3.30
S	0.668	0.690	16.97	17.53
T	0.801	0.821	20.34	20.85
U	0.065	0.080	1.65	2.03

Notes:

1. Pulse test, t ≤ 300µs, duty cycle, d ≤ 2%.
2. Part must be heatsunk for high-temp I_{CES} measurement.
3. Switching times & energy losses may increase for higher V_{CE}(Clamp), T_J or R_G.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2 4,860,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2 4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

Fig. 1. Output Characteristics @ T_J = 25ºC

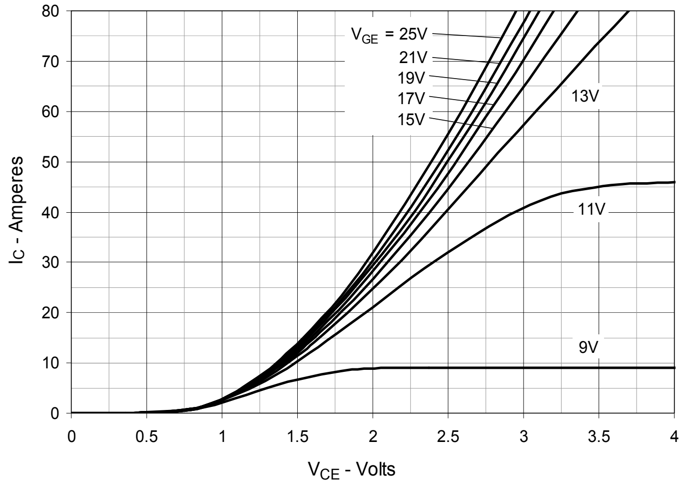


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

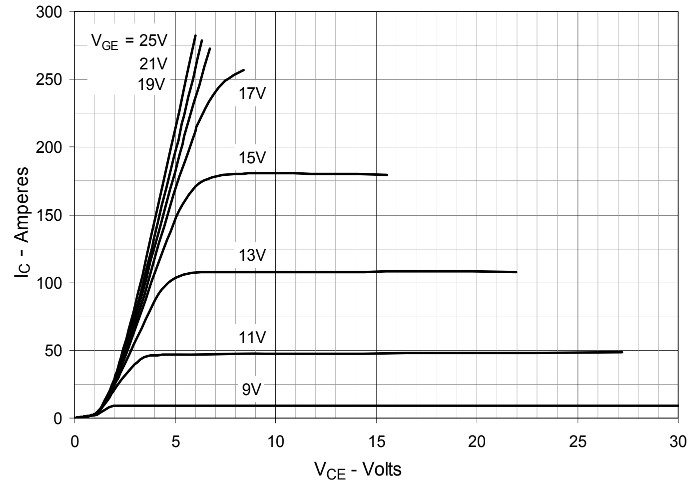


Fig. 3. Output Characteristics @ T_J = 125ºC

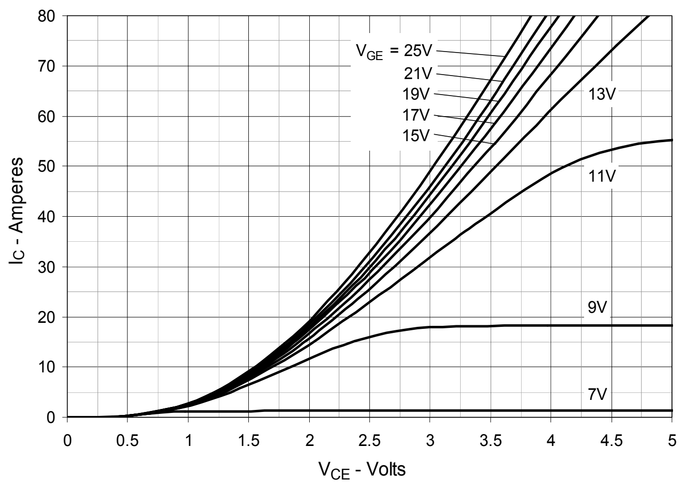


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

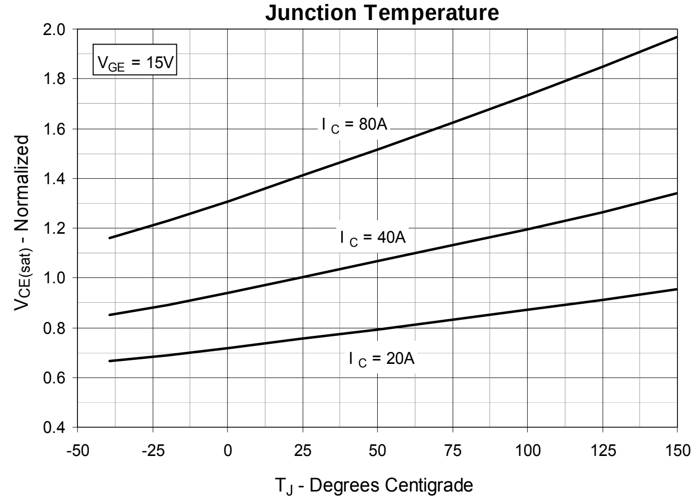


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

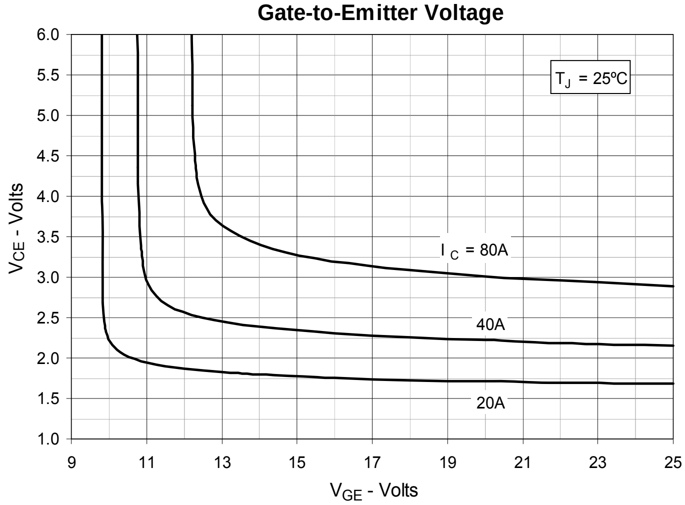


Fig. 6. Input Admittance

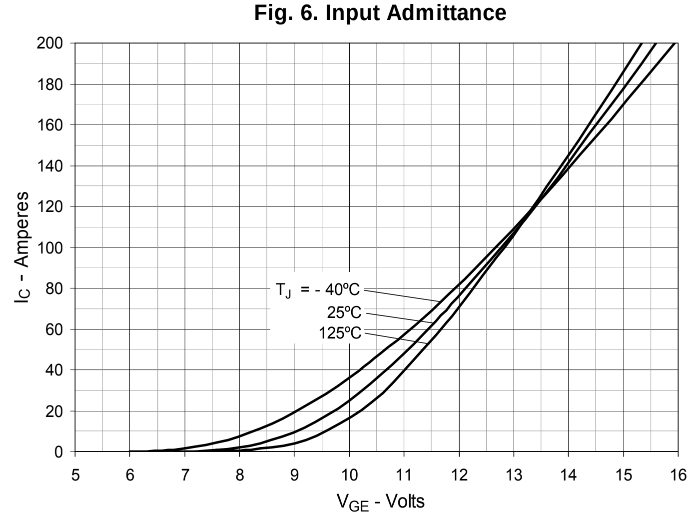


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Fig. 7. Transconductance

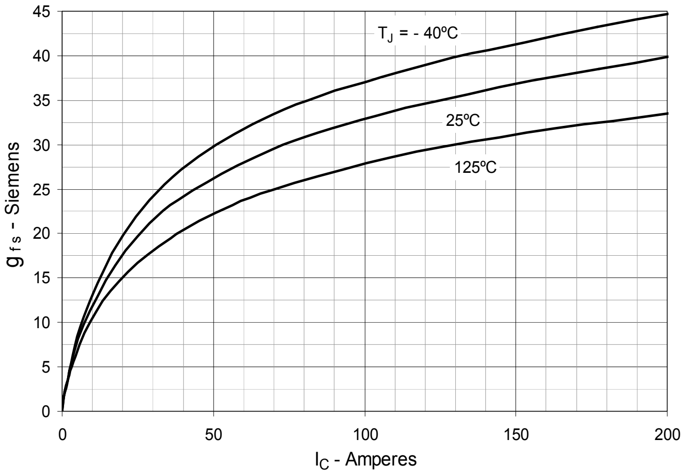

Fig. 8. Gate Charge

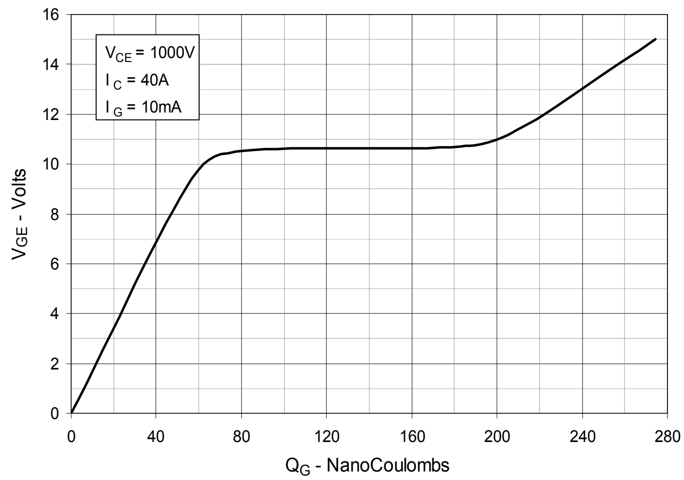

Fig. 9. Capacitance

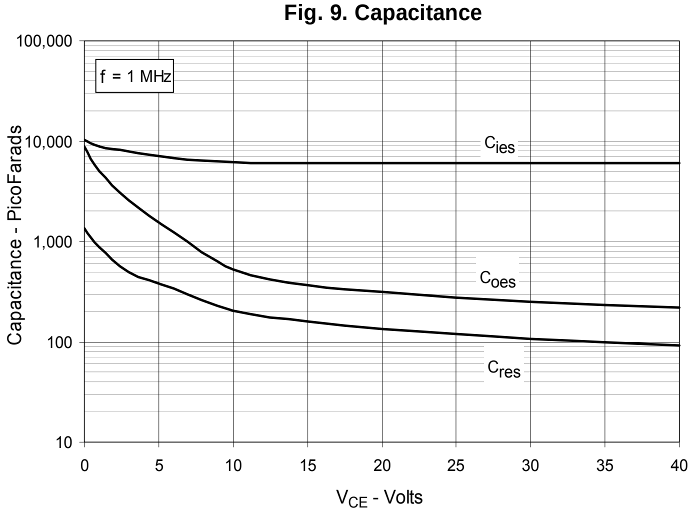

Fig. 10. Reverse-Bias Safe Operating Area

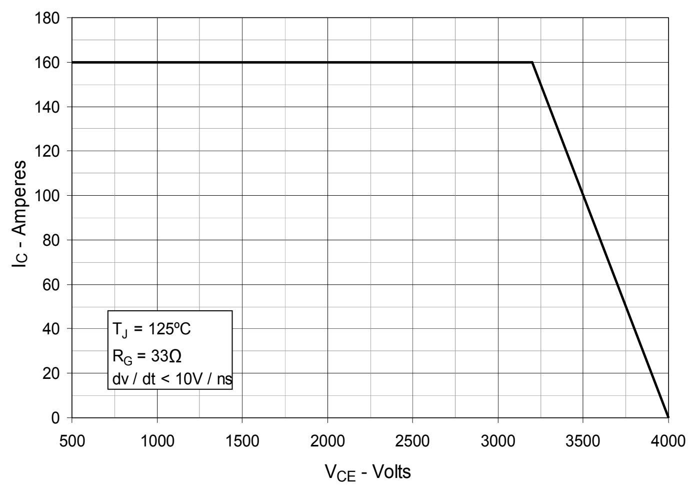

Fig. 11. Maximum Transient Thermal Impedance

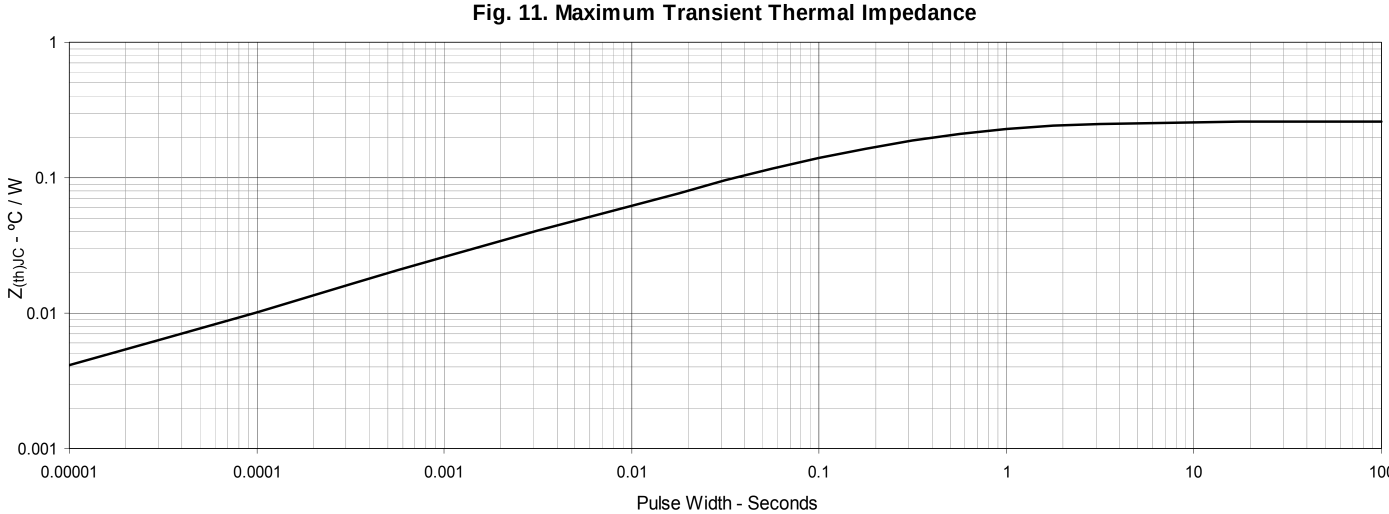

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Fig. 12. Typ. Swicthing Characteristics vs. Collector Current

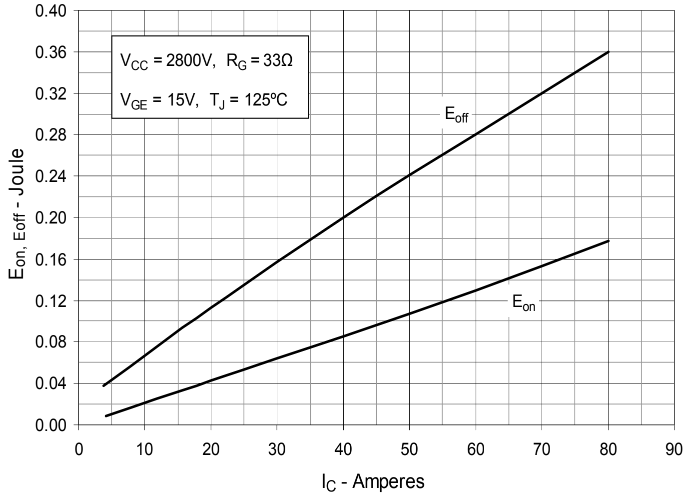
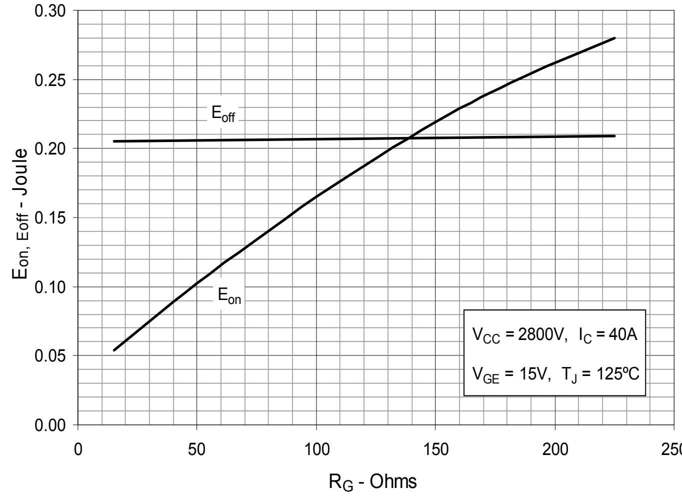


Fig. 13. Typ. Swicthing Characteristics vs. Gate Resistor



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