



### Features

- Bidirectionally Buffers Both I<sup>2</sup>C Signals
- Glitch-Free Operation
- Extends and Isolates I<sup>2</sup>C Interfaces
- Standard- and Fast-mode I<sup>2</sup>C
  - Side B Fast-mode I<sup>2</sup>C Compliant V<sub>DDB</sub> ≥ 4.5V
- Very Low EM and RF Generation - No Internal Clock
- SMBus Compatible V<sub>DDB</sub> = 3.3V
- Operates on 2.7V to 5.5V, Enabling Level Translation
- Slew-Limited Drivers Reduce EMI
- Powerdown to Hi-Z Doesn't Load I<sup>2</sup>C
- 3750V<sub>rms</sub> Galvanic Isolation
- Flammability Rating UL 94 V-0

### Applications

- Isolated Signal Monitoring and Control
- Power-over-Ethernet
- Power Supply High Side Interface
- I<sup>2</sup>C Bus Length Extenders
- I<sup>2</sup>C Logic Level Translation

### Approvals

- UL Recognized Component: File # E76270
- CSA Certified Component: Certificate # 70157867
- TUV EN 62368-1: Certificate # B 082667 0008

### Description

IXYS Integrated Circuits' CPC5902 is a dual, optically isolated, bidirectional logic-bus repeater. It galvanically isolates two open-drain logic signals, and provides a galvanic isolation of 3750V<sub>rms</sub>. When the two sides' supply voltages are configured with different voltages, the CPC5902 also functions as a logic level translator for levels as low as 2.7V or as high as 5.5V.

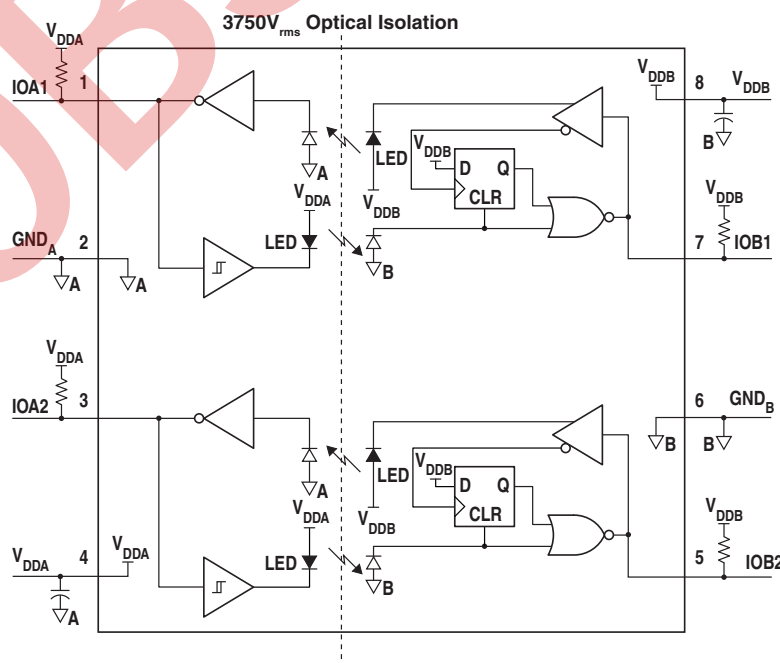
Unlike transformer or capacitive isolators, the optically isolated repeaters pass DC signals, and do not need to be clocked periodically to sustain the logic states. Buffered signals will always return to their proper value after a transient interruption on either side.

### Ordering Information

Part	Description
CPC5902G	8-Pin DIP (50 / Tube)
CPC5902GS	8-Pin Surface Mount (50 / Tube)
CPC5902GSTR	8-Pin Surface Mount (1000 / Reel)



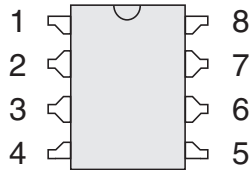
Figure 1. CPC5902 Functional Block Diagram



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## 1 Specifications

### 1.1 Package Pinout



### 1.2 Pin Description

Pin#	Name	Description
1	IOA1	Bidirectional Input/Output 1 - Side A
2	GND <sub>A</sub>	Supply Return - Side A
3	IOA2	Bidirectional Input/Output 2 - Side A
4	V <sub>DDA</sub>	Supply Voltage - Side A
5	IOB2	Bidirectional Input/Output 2 - Side B
6	GND <sub>B</sub>	Supply Return - Side B
7	IOB1	Bidirectional Input/Output 1 - Side B
8	V <sub>ddb</sub>	Supply Voltage - Side B

### 1.3 Absolute Maximum Ratings

Electrical Absolute Maximum Ratings are at 25°C. Voltages with respect to local ground: GND<sub>A</sub> or GND<sub>B</sub>.

Parameter	Symbol	Min	Max	Units
Supply Voltage A	V <sub>DDA</sub>	-0.5	+6.5	V
Supply Voltage B	V <sub>ddb</sub>	-0.5	+6.5	V
Input Voltage	V <sub>IOx</sub>	-0.3	V <sub>DDx</sub> + 0.3	V
Power Dissipation <sup>1</sup>	P <sub>TOT</sub>	-	800	mW
Isolation Voltage, Input to Output				
60 Seconds	-	3750	-	V <sub>rms</sub>
2 Seconds	-	4500	-	
Operating Temperature	T <sub>A</sub>	-40	+85	°C
Operating Relative Humidity (Non-condensing)	RH	5	85	%
Storage Temperature	T <sub>STG</sub>	-50	+125	°C

<sup>1</sup> Derate total power by 7.5mW/°C above 25°C.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

### 1.4 ESD Rating

ESD Rating (Human Body Model)

4000V

### 1.5 Thermal Characteristics

Parameter	Conditions	Symbol	Typical	Units
Thermal Impedance, Junction to Ambient	Free Air	R <sub>θJA</sub>	114	°C/W

### 1.6 General Conditions

Unless otherwise specified, minimum and maximum values are guaranteed by production testing requirements or by design. Typical values are characteristic of the device at 25°C, and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the manufacturing testing requirements.

Specifications cover the operating temperature range  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

### 1.7 Electrical Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Units
<b>Side A</b>						
Supply Voltage	$I_{\text{SINK1}}=6\text{mA}$ , $I_{\text{SINK2}}=6\text{mA}$	$V_{\text{DDA}}$	2.7	-	5.5	V
Supply Current	$V_{\text{DDA}}=3.3\text{V}$ , $I_{\text{SINK}}=0$	$I_{\text{DDA}}$	-	7.5	-	mA
	$V_{\text{DDA}}=3.3\text{V}$ , $I_{\text{SINK1}}=6\text{mA}$ , $I_{\text{SINK2}}=6\text{mA}$		-	7.85	-	
	$V_{\text{DDA}}=5.5\text{V}$ , $I_{\text{SINK}}=0$ , $T_A=25^{\circ}\text{C}$		-	8.1	10	
Leakage Current	$IOA1=IOA2=V_{\text{DDA}}$	$I_{\text{LEAKA}}$	-	0.01	10	$\mu\text{A}$
Input Capacitance		$C_{\text{IN}}$		3		pF
Falling Input Low Threshold	$V_{\text{DDA}}$ 2.7V to 5.5V	$V_{\text{ILA}}$	$0.3V_{\text{DDA}}$	-	-	V
Rising Input High Threshold	$V_{\text{DDA}}$ 2.7V to 5.5V	$V_{\text{IHA}}$	-	-	$0.7V_{\text{DDA}}$	
Hysteresis	$V_{\text{DDA}}=2.7\text{V}$ to 5.5V	$\text{HYST}_A$	-	$0.15V_{\text{DDA}}$	-	V
Output Drive	$V_{\text{DDA}}=2.7\text{V}$ , $I_{\text{SINK}}=3\text{mA}$	$V_{\text{OLA}}$	-	0.21	0.35	V
	$V_{\text{DDA}}=2.7\text{V}$ , $I_{\text{SINK}}=6\text{mA}$		-	0.42	0.7	
Output Temperature Coefficient	$V_{\text{DDA}}=2.7\text{V}$ to 5.5V, $I_{\text{SINK}}=6\text{mA}$	$\text{TC}_A$	-	+1.2	-	$\text{mV}/^{\circ}\text{C}$
<b>Side B</b>						
Supply Voltage	$I_{\text{SINK1}}=I_{\text{SINK2}}=3\text{mA}$	$V_{\text{DDB}}$	2.7	-	5.5	V
Supply Current	$V_{\text{DDB}}=3.3\text{V}$ , $I_{\text{SINK}}=0$	$I_{\text{DDB}}$	-	12.1	-	mA
	$V_{\text{DDB}}=3.3\text{V}$ , $I_{\text{SINK1}}=I_{\text{SINK2}}=3\text{mA}$		-	12.25	-	
	$V_{\text{DDB}}=5.5\text{V}$ , $I_{\text{SINK}}=0$ , $T_A=25^{\circ}\text{C}$		-	12.7	16	
Leakage Current	$IOB1=IOB2=V_{\text{DDB}}$	$I_{\text{LEAKB}}$	-	0.01	10	$\mu\text{A}$
Input Capacitance		$C_{\text{IN}}$		3		pF
Falling Input Low Threshold	$V_{\text{DDB}} = 2.7\text{V}$	$V_{\text{ILB}}$	0.48	0.54	0.6	V
	$V_{\text{DDB}} = 2.7\text{V}$ to 5.5V		$0.2V_{\text{DDB}} - 60\text{mV}$	$0.2V_{\text{DDB}}$	$0.2V_{\text{DDB}} + 60\text{mV}$	
Hysteresis	$V_{\text{DDB}}=2.7\text{V}$ to 5.5V	$\text{HYST}_B$	-	$0.01V_{\text{DDB}}$	-	V
Output Drive	$V_{\text{DDB}}=2.7\text{V}$ , $I_{\text{SINK}}=3\text{mA}$	$V_{\text{OLB}}$	0.63	0.72	0.81	V
	$V_{\text{DDB}}=2.7\text{V}$ , $I_{\text{SINK}}=0.1\text{mA}$		-	0.62	-	
	$V_{\text{DDB}} = 2.7\text{V}$ to 5.5V, $I_{\text{SINK}}=3\text{mA}$		-	$0.23V_{\text{DDB}}$	$0.23V_{\text{DDB}} + 190\text{mV}$	
	$V_{\text{DDB}} \geq 4.5\text{V}$ , $I_{\text{SINK}}=6\text{mA}$		-	-	$0.3V_{\text{DDB}}$	
Self-Drive Margin	$V_{\text{DD}}=2.7\text{V}$ , $I_{\text{SINK}}=0.1\text{mA}$ (Self_Out-In) $V_{\text{DIFFERENCE}}$	$V_{\text{OLB}} - V_{\text{ILB}}$	25	-	-	mV
Output Temperature Coefficient	$V_{\text{DDB}}=2.7\text{V}$ to 5.5V, $I_{\text{SINK}}=3\text{mA}$	$\text{TC}_B$	-	+0.4	-	$\text{mV}/^{\circ}\text{C}$

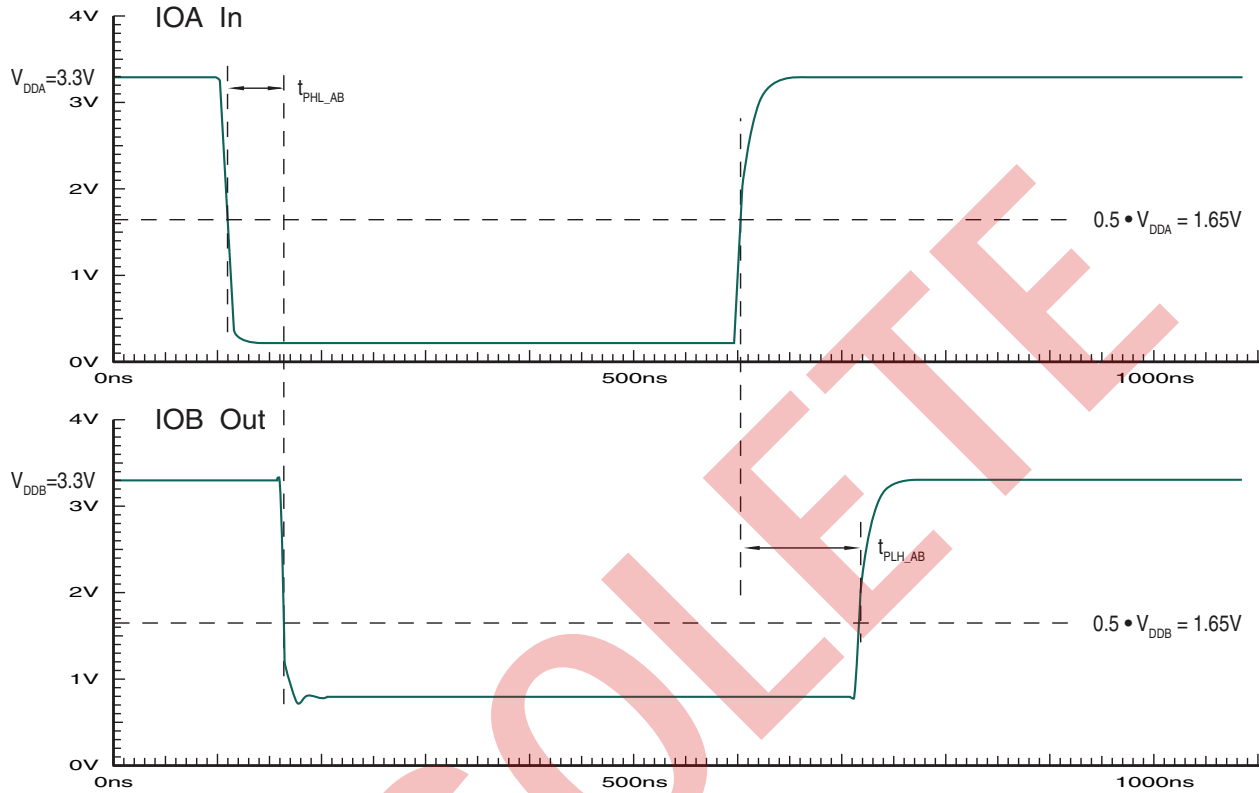
### 1.8 Switching Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Units	
I <sup>2</sup> C Clock Frequency	I <sub>SINKA</sub> =6mA, C <sub>LOADA</sub> =400pF	I <sub>SINKB</sub> =3mA, C <sub>LOADB</sub> =200pF	f <sub>MAX</sub>	500	-	-	kHz
		I <sub>SINKB</sub> =6mA, C <sub>LOADB</sub> =400pF (V <sub>DDB</sub> ≥ 4.5V)					
Propagation Delay A to B <sup>1</sup> Falling Rising	V <sub>DDA</sub> =V <sub>DDB</sub> =3.3V, R <sub>PUA</sub> =475Ω, R <sub>PUB</sub> =825Ω, C <sub>IOA</sub> =C <sub>IOB</sub> =20pF	0.5V <sub>DDA</sub> to 0.5V <sub>DDB</sub>	t <sub>PHL_AB</sub>	-	60	135	ns
			t <sub>PLH_AB</sub>	-	122	270	
Propagation Delay B to A <sup>2</sup> Falling Rising	V <sub>DDA</sub> =V <sub>DDB</sub> =3.3V, R <sub>PUA</sub> =475Ω, R <sub>PUB</sub> =825Ω, C <sub>IOA</sub> =C <sub>IOB</sub> =20pF	0.2V <sub>DDB</sub> to 0.5V <sub>DDA</sub>	t <sub>PHL_BA</sub>	-	90	170	ns
			t <sub>PLH_BA</sub>	-	165	275	
Propagation Delay B to A to B <sup>2</sup> Rising		0.2V <sub>DDB</sub> to 0.5V <sub>DDB</sub>	t <sub>PLH_BAB</sub>	-	290	480	ns

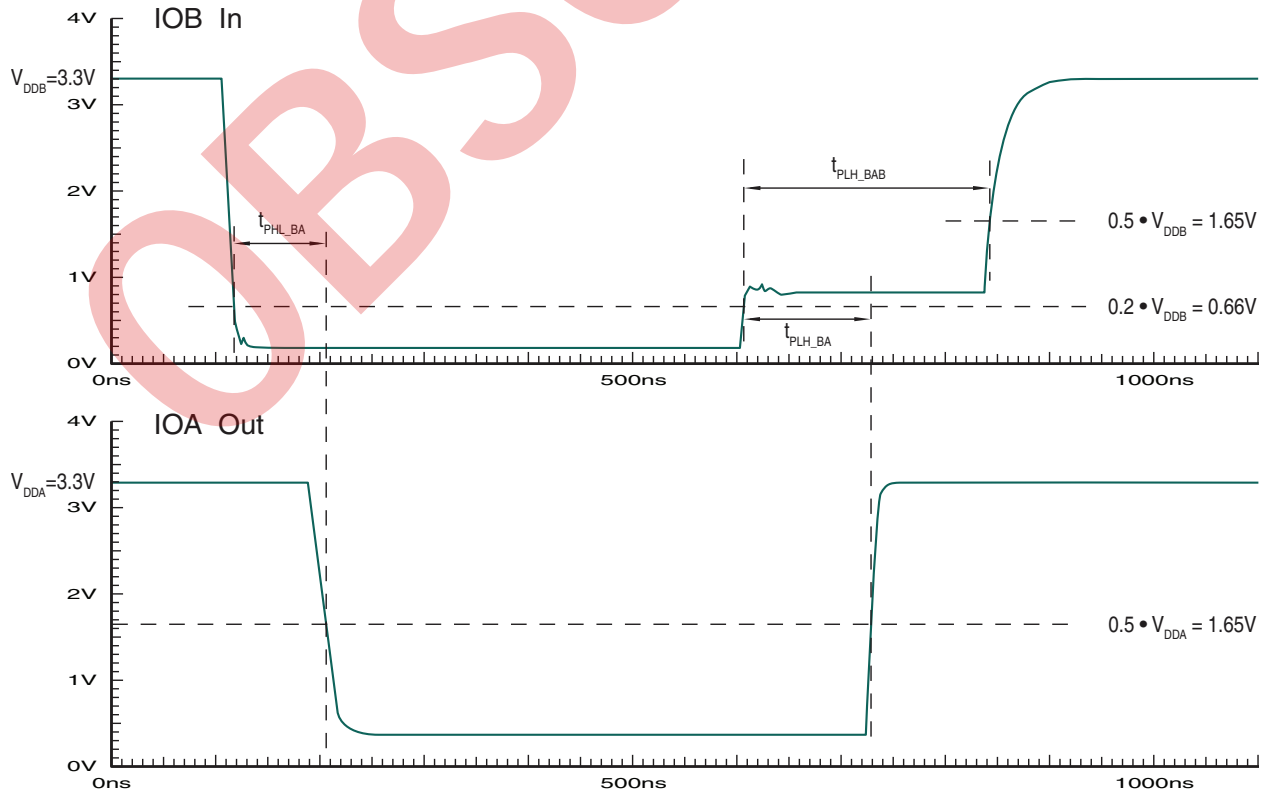
<sup>1</sup> Refer to "IOA to IOB Switching Waveforms" on page 6

<sup>2</sup> Refer to "IOB to IOA Switching Waveforms" on page 6

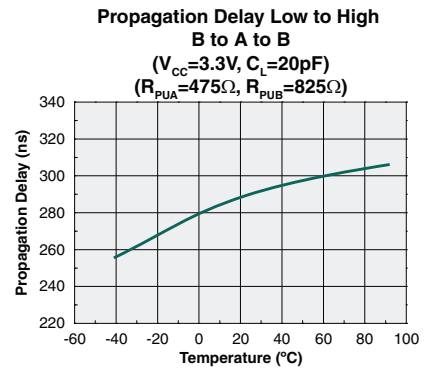
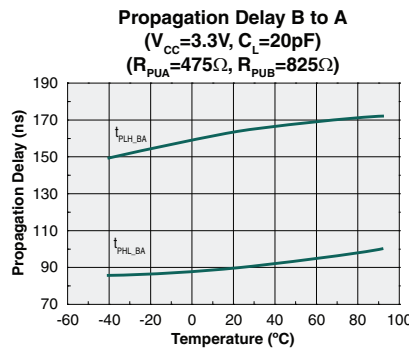
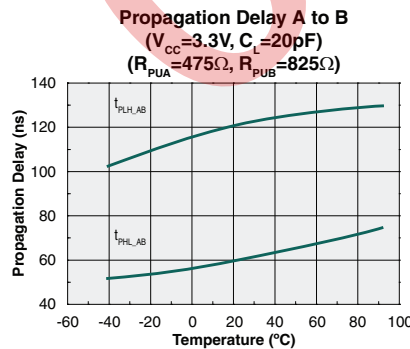
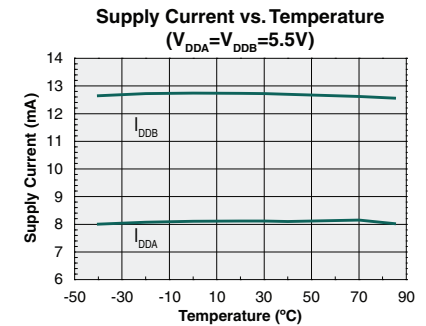
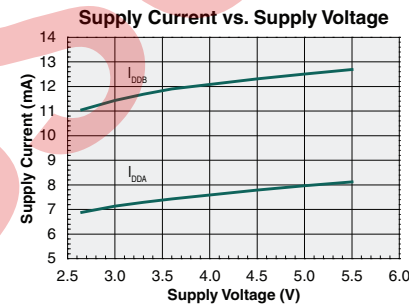
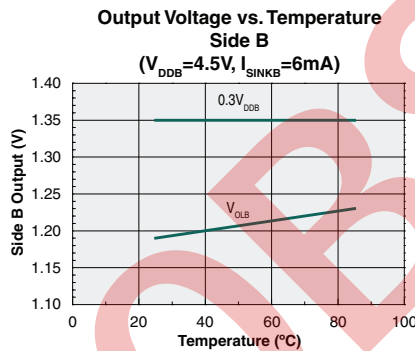
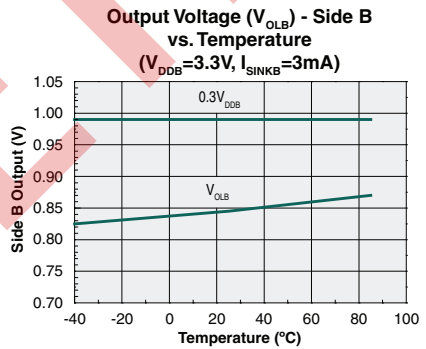
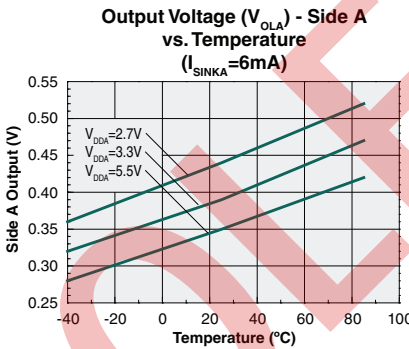
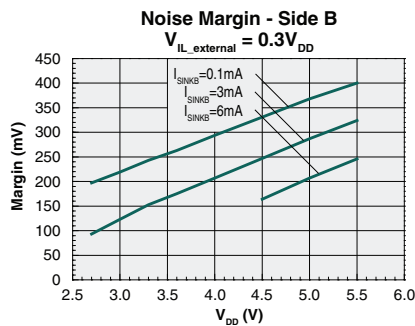
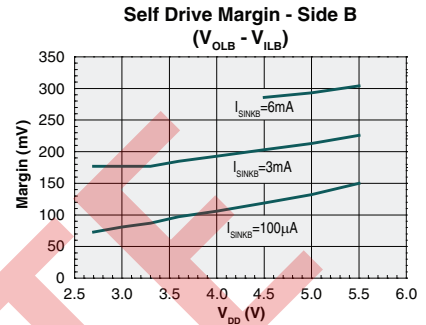
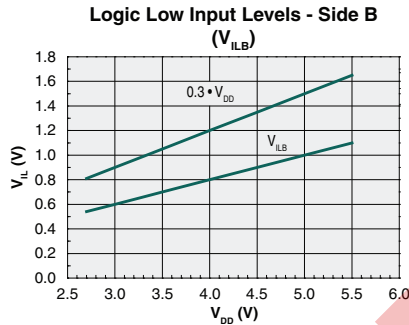
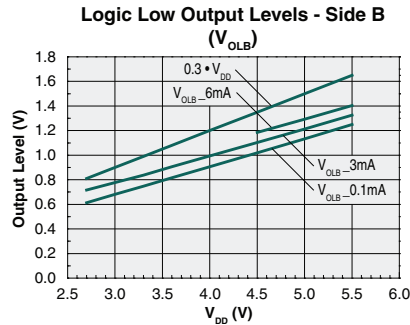
1.9 IOA to IOB Switching Waveforms



1.10 IOB to IOA Switching Waveforms



## 2 Performance Data\*



\*Unless otherwise noted, data presented in these graphs is typical of device operation at 25°C. For guaranteed parameters not indicated in the written specifications, please contact our applications department.

### 3 Functional Description

#### 3.1 Overview

The CPC5902 combines the features of multiple logic optoisolators and an I<sup>2</sup>C bus repeater in a single 8-pin package. It offers excellent isolation (3750V<sub>rms</sub>) and speed sufficient to support I<sup>2</sup>C Fast-mode at 400kbps. It bidirectionally buffers the two I<sup>2</sup>C signals across the isolation barrier, and supports I<sup>2</sup>C clock stretching. If different supply voltage levels are used at each side, then the part, in conjunction with its external pullup resistors, will perform logic level translation for V<sub>DD</sub> between 2.7V and 5.5V at either side.

The CPC5902, like available non-galvanically isolating I<sup>2</sup>C bus repeaters, has a full drive side and a limited drive side. It uses a voltage-limited output driver and a lower V<sub>THRESHOLD</sub> (V<sub>IL</sub>) at the Side B IO. The voltage-limited Side B output driver can not output a V<sub>OL</sub> level below an internally set voltage limit. This is necessary to ensure that the CPC5902 cannot drive its own IOB input to a level it accepts as a logic low, which would cause I<sup>2</sup>C bus contention. The parts are specified with a minimum V<sub>OL</sub>-V<sub>IL</sub> margin of 25mV at minimum V<sub>DDB</sub>, and exhibit a proportionately larger self-drive margin with larger V<sub>DDB</sub>.

The Side A drivers are Fast-mode, full strength (6mA) over the full V<sub>DDA</sub> range, and the input thresholds are specified to be Fast-mode compliant; thus Side A will drive up to the full 400pF Fast-mode C<sub>LOAD</sub> and is allowed to drive its own input to a logic low. Devices meeting the I<sup>2</sup>C specification are easily able to drive the IO nodes below the CPC5902's lower V<sub>IL</sub> (0.2V<sub>DDB</sub>) threshold at the Side B inputs, and will correctly accept the CPC5902 Side B driven data, thereby enabling Side B bidirectional communication at up to 3mA of load current over the full V<sub>DDB</sub> range.

Over the entire V<sub>DDx</sub> range, Side A is fully I<sup>2</sup>C

Fast-mode compliant while Side B is I<sup>2</sup>C Standard-mode compliant. It is important to note that Side B can be operated at the Fast-mode data rate when the capacitive loading on the bus is kept at 200pF or less, however when V<sub>DDB</sub> ≥ 4.5V, Side B is also Fast-mode compliant with up to 400pF capacitive loading.

determined by t<sub>OPLH\_AB</sub>. Side B deassertion occurs at

IO pullup resistors are required on both sides of the barrier. At the Side B inputs, resistor values should be chosen for Standard-mode 3mA pullup current (for operation independent of V<sub>DDB</sub>). Pullups chosen for Fast-mode drivers (up to 6mA) can be used at Side A with no loss of noise margin.

Applying a pulse at a Side B input inherently involves the use of some of the output driver circuits at that I/O. In a manner similar to the I<sup>2</sup>C clock stretching feature, once an asserted signal is determined to be valid, it is stretched until its proper transmission through the optics has been verified. This insures that there will be no extra edges generated at either side due to optic delays. If a Side B asserted-low pulse is long enough to be accepted and passed to Side A, then the flip-flop at Side B is set and remains set until the signal returns through the optics from Side A.

In operation, a valid asserted pulse of less than 80ns applied at Side B appears at Side A after a delay largely determined by the low-pass filter delay (t<sub>FIL</sub>) and the optics delay (t<sub>OPLH\_BA</sub>). After this initial delay the Side A driver is activated and a logic low is asserted at time:

$$t_{STARTA} = t_{FIL} + t_{OPLH\_BA}$$

That assertion is returned across the optics to Side B after a delay largely determined by t<sub>OPLH\_AB</sub>. Upon arriving at Side B, the flip-flop is cleared, and the deassertion is sent through the optics to Side A, arriving at the Side A output after a delay largely determined by t<sub>OPLH\_BA</sub> at time:

$$t_{ENDA} = t_{FIL} + t_{OPLH\_BA} + t_{OPLH\_AB} + t_{OPLH\_BA}$$

Thus a valid Side B pulse having a width less than 80ns is stretched at Side A to a typical width of 125ns. The duration of the pulse width output onto the Side A bus is given by:

$$t_{PWA\_min} = (t_{OPLH\_AB} + t_{OPLH\_BA})$$

When Side A is deasserted, the output rises at a slew rate determined by the RC load on IOA, and passes the logic threshold after time t<sub>SLEWA</sub>. The deasserted (logic HIGH) input propagates through the optics and deasserts the Side B output after a delay largely

time t<sub>ENDB</sub> given by:



$$t_{ENDB} = t_{ENDA} + t_{SLEWA} + t_{OPLH\_AB}$$

Thus at Side B input, an applied pulse of less than 80ns is stretched to:

$$t_{PWB\_min} = t_{FIL} + t_{OPLH\_BA} + t_{OPLH\_AB} + t_{OPLH\_BA} + t_{SLEWA} + t_{OPLH\_AB}$$

which is typically 330ns. More importantly, only one pulse is seen at both ports, with no extra or missing clock or data edges, assuring line integrity.

Pulses of width larger than approximately 80ns applied to the Side B input do not utilize the flip-flop to terminate the pulse, but do need to propagate to Side A and then back to Side B when returning high after being asserted low. The Side A pulse width is given by the usual pulse width distortion relation:

$$t_{PWA\_nom} = t_{PULSE} + t_{PLH\_BA} - t_{PHL\_BA}$$

which is typically  $t_{PULSE} + 75ns$ . Note that  $t_{PLH\_BA}$  and  $t_{PHL\_BA}$  are observed at the external pins, and are provided in the table, **“Electrical Specifications” on page 4**. The pulse at Side B is asserted by an external driver pulling low, and lasts for time  $t_{PULSE}$ . At the end of the pulse, the rising edge passes through the internal filter with delay  $t_{FIL}$ , then applied to the LED and received at Side A  $t_{OPLH\_BA}$  later. After time  $t_{SLEWA}$  the output at Side A crosses the logic high threshold causing the Side A LED drive to deactivate, which propagates the deasserted state back to Side B with a delay of  $t_{OPLH\_AB}$ . Thus normal-width pulses of width  $t_{PULSE}$  applied at Side B (IOB) exhibit a stretched pulse width of:

$$t_{PWB\_nom} = t_{PULSE} + t_{FIL} + t_{OPLH\_BA} + t_{SLEWA} + t_{OPLH\_AB}$$

at IOB, which is also given by:

$$t_{PWB\_nom} = t_{PULSE} + t_{PHL\_BAB}$$

and is typically  $t_{PULSE} + 290ns$ .

Side A receivers have been designed to exhibit a significant amount of hysteresis, which helps to eliminate false clocking. They have not been internally low-pass filtered beyond the filtering inherent within the optical channel. When the I<sup>2</sup>C bus is terminated for maximum bandwidth (6mA pullups and minimal capacitance), the receivers typically will respond to pulses greater than 12ns. If additional filtering is desired, then externally increasing the load capacitance of the I<sup>2</sup>C lines until the amount of time the offending signal spends above/below  $V_{DD}/2$  is

less than 10ns will reject the signal at the expense of increasing rise and fall times.

Side B receivers do implement some hysteresis and low-pass filtering in addition to the optics. An asserted pulse typically needs to be held below  $0.2V_{DD}$  for 15ns before it is accepted at Side B input. This may require a 30ns pulse applied by a typical driver with just 20pF loading the I<sup>2</sup>C lines.

While any very short pulses stretched to the minimum times above would seem to cause large amounts of pulse width distortion, within 400kHz Fast-mode I<sup>2</sup>C the shortest allowable signal or clock asserted low time is 1.3 $\mu$ s. Neither Standard-mode nor Fast-mode variants include any legal signals that are less than 80ns (typ); thus the  $t_{PWA\_nom}$  and  $t_{PWB\_nom}$  equations above always apply. The pulse width on valid longer pulses receives less stretching and is proportionally less noticeable. For example the Fast-mode minimum clock low time of 1.3 $\mu$ s when applied at Side B would typically be seen as a 1.375 $\mu$ s pulse at Side A and will be stretched to a length of 1.59 $\mu$ s for other devices on the Side B bus.

Internal filtering and the flip-flop at Side B are used to ensure that an equal number of pulse edges are seen at both sides of the isolation barrier when Side B is driven. When a signal at Side B is asserted low, the flip-flop self-drives that Side B I/O pin until the optical channel back from Side A proves that Side A has successfully been asserted. While this is generally a welcome error reduction feature and is especially useful on the side with nonstandard levels, it does need to be considered when assigning Side A and Side B ports. If Side A is not powered up, then the signal back from Side A will not appear until after Side A has been powered, and the signal at Side B will be stretched until that time. Side A uses filtered hysteresis at its standard inputs, not pulse stretching, to defeat sub-minimum-size pulses. Thus that side of the isolation barrier, which will be the bus master at power-up, should generally be assigned to Side A.

Note that the pinout of the package is rotationally symmetrical. As a result, changing which side of the isolation barrier utilizes Side A standard levels can be accomplished by rotating the part 180° before it is soldered onto the board.

### 3.2 Calculating Minimum Pull-Up Resistor Values

The minimum value of the pull-up resistor,  $R_{PU}$ , on the I<sup>2</sup>C bus is chosen based upon the expected  $V_{DD}$  supply voltage range and the weakest load current sinking device on the bus. Note: Systems that do not need maximum bandwidth and busses with lower capacitive loading can use a higher value for the pull-up resistor to reduce power consumption.

#### 3.2.1 Side A Pull-Up Resistor: $R_{PUA}$

The weakest I<sup>2</sup>C compliant device on the Side A bus, with  $R_{PUA}$  to  $V_{DDA}$ , must be able to pull the Side A inputs below 0.4V for outputs rated at 3mA or 0.6V for outputs rated at 6mA when  $V_{DDA}$  is at its maximum.

For example, if the weakest device is only guaranteed to sink 3mA then the maximum allowed logic low output voltage will be 0.4V. For designs with  $V_{DDA\_max} = 3.6V$ , the minimum voltage across the pull-up resistor is:

$$\text{Minimum } R_{PUA} \text{ Voltage} = 3.6 - 0.4 = 3.2V$$

For the I<sup>2</sup>C minimum current sink requirement of 3mA, the minimum value of the pull-up resistor is easily calculated as:

$$R_{PUA\_min} = 3.2V / 3mA = 1066.7\Omega$$

Chose a standard value resistor that will not violate this minimum value over tolerance and temperature, such as a 1.1k $\Omega$ , 1% tolerance, 100ppm/ $^{\circ}C$  temperature coefficient resistor.

If all the non-CPC5902 devices on the Side A bus are Fast-mode compliant (400pF capacitive loading capable) with the required 6mA current sink capability, then the bus can be configured for Fast-mode. Resistor selection for Fast-mode is similar to the example given above but because the logic low output level is greater (0.6V) then the voltage across the pull-up resistor will be less. Calculation of the compliant Fast-mode bus minimum pull-up resistor value is given by:

$$R_{PUA\_min} = (3.6 - 0.6)V / 6mA = 500\Omega$$

The minimum E96 standard value 1% tolerance, 100ppm/ $^{\circ}C$  temperature coefficient resistor is 511 $\Omega$ .

#### 3.2.2 Side B Pull-Up Resistor: $R_{PUB}$

Calculating the pull-up resistor for Side B is similar to the process used for Side A but with some additional considerations.

Before proceeding, it must be pointed out that Side B of the CPC5902 is Fast-mode compliant with  $V_{DDB} \geq 4.5V$ . This means the CPC5902 Side B outputs are 6mA capable allowing bus operation of 400kb/s with up to 400pF of capacitive loading. For  $V_{DDB}$  supply levels below 4.5V the CPC5902 outputs are only rated for 3mA but can be operated at Fast-mode speeds of 400kb/s whenever the bus capacitive loading  $C_{LOAD} \leq 200pF$ . Greater capacitive loading of the Side B bus limits the CPC5902 to data rates of 100kb/s.

First, it must be determined if the Side B bus will be configured for 3mA or 6mA operation. This is done by evaluating the external (non-CPC5602) devices on the Side B bus and the operational capabilities of the CPC5902. There are three possibilities:

- 1) One or more of the external devices is limited to 3mA of output current sink.
- 2) All of the external devices are rated at 6mA of output current sink and the Side B minimum supply voltage  $V_{DDB} < 4.5V$ .
- 3) All of the external devices are rated at 6mA of output current sink and the Side B minimum supply voltage  $V_{DDB} \geq 4.5V$ .

For conditions 1 and 2 above the bus must be configured for 3mA. Condition 3 is the only situation where the bus can be configured for 6mA, a Fast-mode requirement when capacitive bus loading is an issue.

Second, it is necessary to configure the Side B bus to be compatible with the CPC5902's lower logic low input threshold:

$$V_{ILB} = 0.2 \cdot V_{DDB} - 60mV$$

As discussed earlier, this lower input threshold requirement is to ensure the CPC5902 can drive a logic low output that is recognized by the other I<sup>2</sup>C devices on the bus, but will not accept it's own logic low output. This prevents latching of the CPC5902. Additionally, this implies there can be no more than one limited drive (Side B) CPC5902 interface on the Side B bus, and that all other devices on the Side B bus must have  $V_{IL} = 0.3 \cdot V_{DDB}$  logic low input thresholds. Because the CPC5902 Side A inputs are compatible with this requirement, any number of

CPC5902 Side A devices may be connected to the Side B bus.

For all modes, the minimum required voltage drop across the Side B pull-up resistor at  $V_{DDB\_max}$  by the external non-CPC5902 I<sup>2</sup>C bus drivers is:

$$\begin{aligned} \text{Minimum } R_{PUB} \text{ Voltage} &= V_{DDB\_max} - (0.2 \cdot V_{DDB\_max} - 60\text{mV}) \\ &= 0.8 \cdot V_{DDB\_max} + 60\text{mV} \end{aligned}$$

which gives the calculation for the minimum value of the pull-up resistor as:

$$R_{PUB\_min} = (0.8 \cdot V_{DDB\_max} + 60\text{mV}) / I_{OL}$$

where  $I_{OL}$  is the guaranteed logic low drive current of the non-CPC5902 bus drivers.

For Standard-mode designs, with output drivers rated at 3mA and a maximum supply voltage of 3.6V, the minimum value of the pull-up resistor is:

$$R_{PUB\_min} = (0.8 \cdot 3.6 + 60\text{mV}) / 3\text{mA} = 980\Omega$$

The minimal standard value 1% resistor with a 100ppm/°C temperature coefficient that will not go below the calculated minimum due to tolerance and temperature is 1kΩ.

In Fast-mode designs with 6mA capable output drivers and a supply voltage maximum of 5.5V, the minimum Fast-mode pull-up resistor value is calculated to be:

$$R_{PUB\_min} = (0.8 \cdot 5.5 + 60\text{mV}) / 6\text{mA} = 743.3\Omega$$

For a Fast-mode design with high capacitive bus loading a 768Ω, 1%, 100ppm/°C resistor would suffice. When the bus does not have a heavy capacitive load then a larger value pull-up resistor can be used thereby reducing overall power consumption.

## 4 Manufacturing Information

### 4.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
CPC5902GS	MSL 3

### 4.2 ESD Sensitivity



This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

### 4.3 Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature ( $T_C$ ) and the maximum total dwell time ( $t_p$ ) in all reflow processes that the body temperature of these surface mount devices may be ( $T_C - 5$ )°C or greater. The device's body temperature must not exceed the Classification Temperature at any time during reflow soldering processes.

Device	Classification Temperature ( $T_C$ )	Dwell Time ( $t_p$ )	Max Reflow Cycles
CPC5902GS	250°C	30 seconds	3

For through-hole devices, the maximum pin temperature and maximum dwell time through all solder waves is provided in the table below. Dwell time is the interval beginning when the pins are initially immersed into the solder wave until they exit the solder wave. For multiple waves, the dwell time is from entering the first wave until exiting the last wave. During this time, pin temperatures must not exceed the maximum temperature given in the table below. Body temperature of the device must not exceed the limit shown in the table below at any time during the soldering process.

Device	Maximum Pin Temperature	Maximum Body Temperature	Maximum Dwell Time	Max Reflow Cycles
CPC5902G	260°C	250°C	10 seconds*	1

\*Total cumulative duration of all waves.

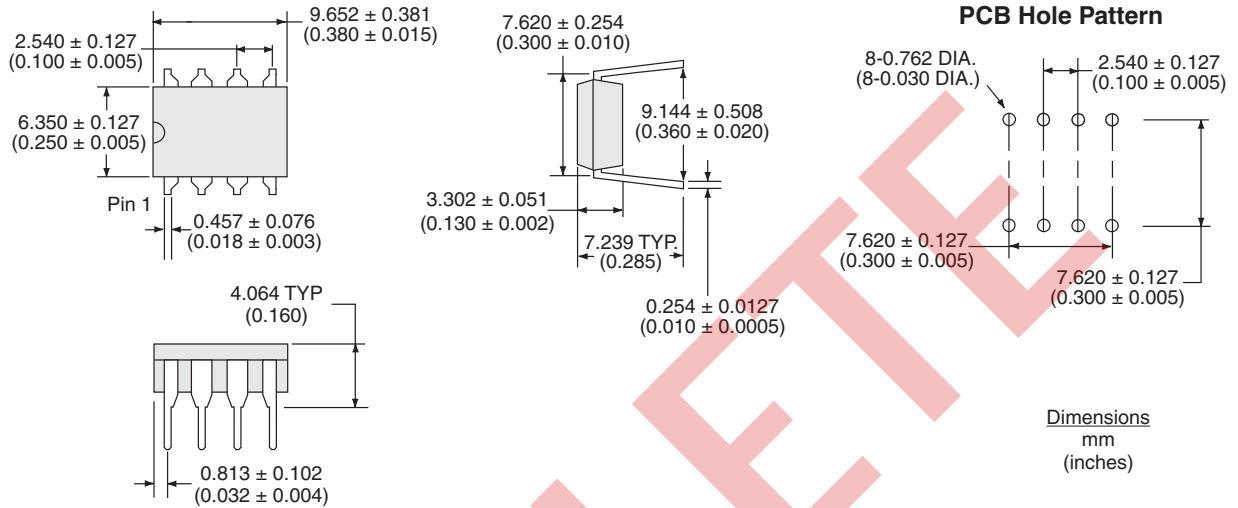
### 4.4 Board Wash

IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

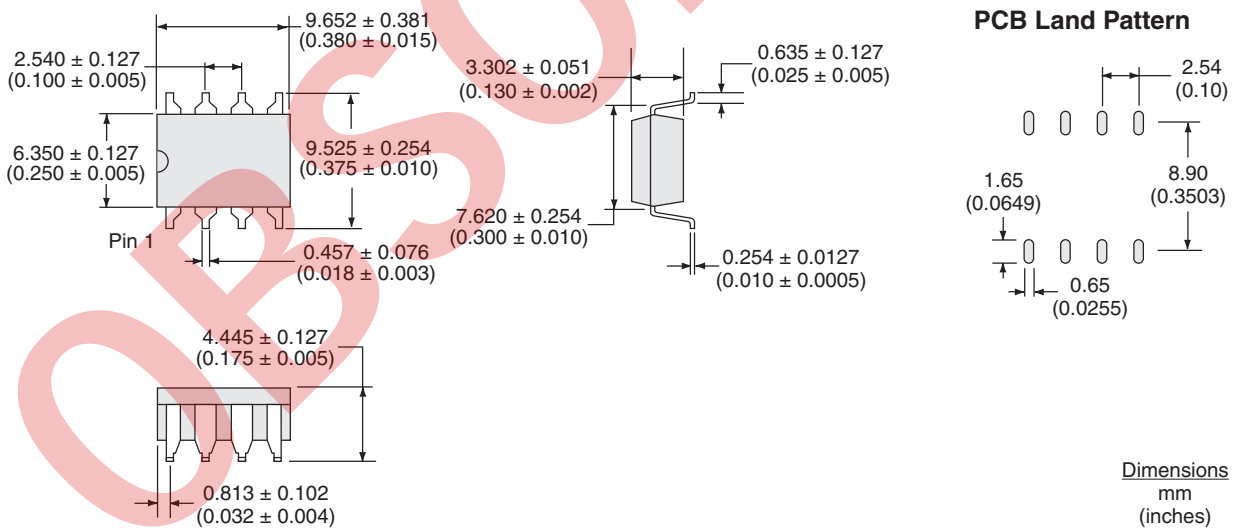


4.5 Mechanical Dimensions

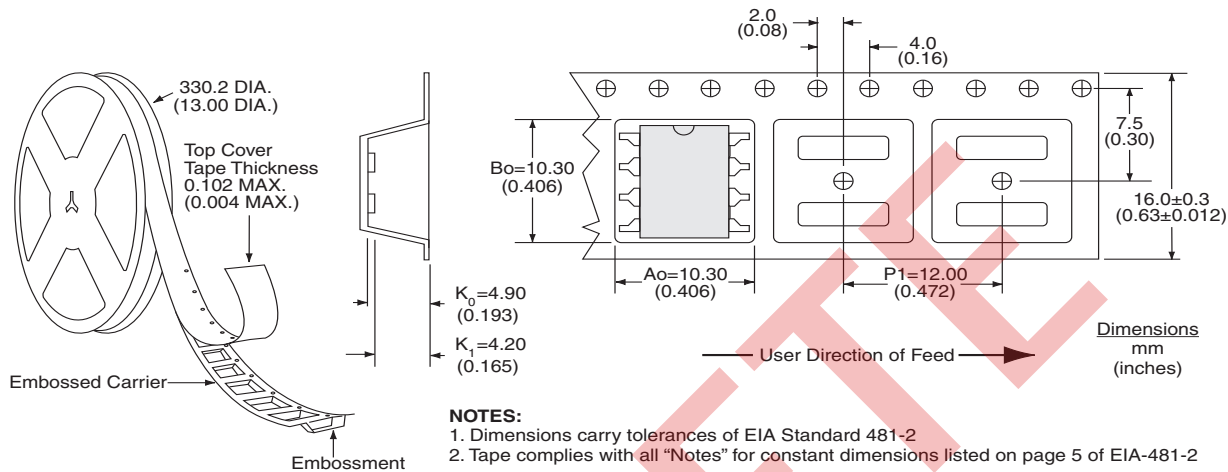
4.5.1 CPC5902G Package



4.5.2 CPC5902GS Package



4.5.3 CPC5902GSTR Tape & Reel Packaging



For additional information please visit our website at: <https://www.ixysic.com>



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