



Features

- Dual Optical Isolator
- Buffers Two Independent Signals
- Power-Down to Hi-Z Doesn't Load Outputs
- Low-Power CMOS Reduces Supply Current
- Output operates Over $2.7V < V_{DD} < 5.5V$
- LED Drive Current Only 1.5mA
- High Speed: 10Mbaud Typical
- 3750V_{rms} Galvanic Isolation
- Single 8-Pin DIP or Surface Mount Package
- Flammability Rating UL 94 V-0

Applications

- Test and Measurement
- A/D and D/A Isolation
- Power Converter Isolation
- Medical
- Ground Loop Elimination
- I²C Bus Isolation
- Computer Bus Isolation
- Isolated Line Receiver

Approvals

- UL Recognized Component: File # E76270
- CSA Certified Component: Certificate # 70157867
- TUV EN 62368-1: Certificate # B 082667 0008



Description

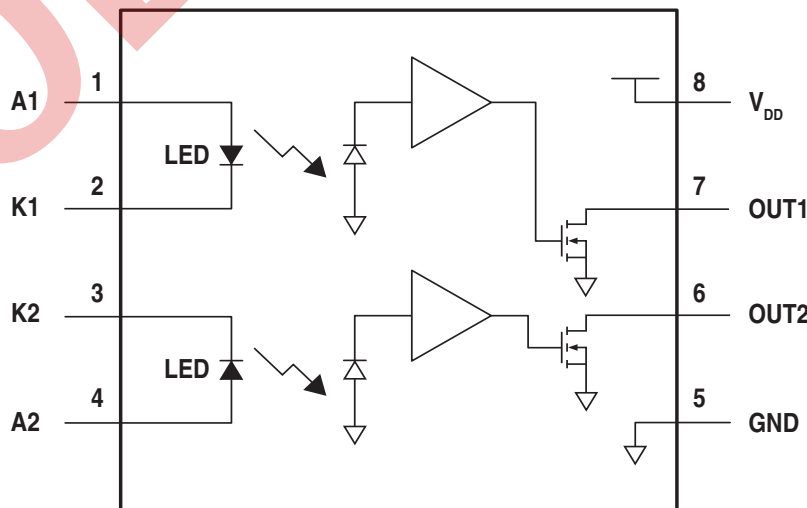
The CPC5002 is a dual high speed optical logic isolator with open-drain outputs providing 3750V_{rms} of galvanic isolation between the inputs and the outputs. Activating the input LED causes the open-drain output to turn on, pulling the voltage of the external pullup resistor towards ground. Utilizing CMOS technology enables the output stage's high-gain circuitry to operate with a miserly power consumption of <5mW (typical) when operated with a 3.3V supply voltage and a low input LED drive current of 1.5mA.

Because optical isolators pass logic levels directly there is no internal state refresh clock to maintain a non-changing input. Additionally, the CPC5002 will always return the buffered signals to their proper value after a transient interruption at either side.

Ordering Information

Part	Description
CPC5002G	8-Pin DIP (50 / Tube)
CPC5002GS	8-Pin Surface Mount (50 / Tube)
CPC5002GSTR	8-Pin Surface Mount Tape & Reel (1000 / Reel)

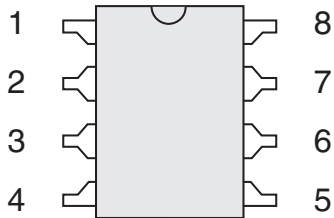
Figure 1. CPC5002 Functional Block Diagram



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1 Specifications

1.1 Package Pinout



1.2 Pin Description

Pin#	Name	Description
1	A1	LED Anode, Channel 1
2	K1	LED Cathode, Channel 1
3	K2	LED Cathode, Channel 2
4	A2	LED Anode, Channel 2
5	GND	Ground, Output Side Supply Return
6	OUT2	Output, Channel 2
7	OUT1	Output, Channel 1
8	V _{DD}	Supply Voltage, Output Side

1.3 Absolute Maximum Ratings

Voltages at Output Side nodes are with respect to GND=0V

Parameter	Symbol	Rating	Units
LED Forward Current Continuous	I _F	20	mA
Peak		40	
LED Input Power (Each)	P _{IN}	72	mW
LED Reverse Voltage	V _R	6.5	V
Supply Voltage, Output Side	V _{DD}	-0.3 to 6.5	V
Output Voltage	V _{OUT}	-0.3 to 6.5	V
Output Current	I _{OUT}	10	mA
Output Power (Each Output)	P _{OUT}	65	mW
Isolation Voltage (Input to Output)	V _{ISO}	3750	V _{rms}
Operating Temperature	T _A	-40 to 85	°C
Operating Relative Humidity	RH	5 to 85	%
Storage Temperature	T _{STG}	-50 to 125	°C

Absolute maximum electrical ratings are at 25°C. Power specifications: no derating required to 85°C.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 ESD Rating

ESD Rating (Human Body Model)

4000V

1.5 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{DD}	2.7	-	5.5	V
LED Forward Current	I_F	1.4	1.5	10	mA
Output Drive	I_{SINK}			6	mA
Operating Ambient Temperature	T_A	-40		+85	°C

1.6 General Conditions

Specifications cover the operating temperature range $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ and supply range $V_{DD} = 2.7\text{V}$ to 5.5V . Unless otherwise specified, minimum and maximum values are guaranteed by production testing. Typical values are the result of engineering evaluations and are characteristic of the device at $T_A = 25^{\circ}\text{C}$ and $V_{DD} = 3.3\text{V}$; they are provided for information purposes only and are not verified by manufacturing testing.

1.7 Electrical Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Specifications						
LED Input Threshold Current	-	I_{TH}	0.16	0.55	1	mA
LED Forward Voltage	$I_F=1.5\text{mA}$, $T_A=25^{\circ}\text{C}$ $I_F=10\text{mA}$	V_F	0.98	1.2	1.41	V
			1.0	1.3	1.8	
LED Reverse Breakdown Voltage	$I_R=5\mu\text{A}$	V_R	6	-	-	V
LED Capacitance	$V_F=0\text{V}$, $f=1\text{MHz}$	C_{IN}	-	50	-	pF
Output Specifications						
Output Drive	$V_{DD}=2.7\text{V}$, $I_{SINK}=3\text{mA}$	V_{OL}	-	0.21	0.35	V
	$V_{DD}=2.7\text{V}$, $I_{SINK}=6\text{mA}$		-	0.42	0.7	
	$V_{DD}=3.3\text{V}$, $I_{SINK}=6\text{mA}$		-	0.38	-	
High Level Leakage Current	$V_{OUT}=V_{DD}=5.5\text{V}$	I_{OHL}	-	0.1	10	μA
Supply Specifications						
Supply Current	$V_{DD}=3.3\text{V}$, $I_{SINK}=0\text{mA}$	I_{DD}	-	1.4	-	mA
	$V_{DD}=5.5\text{V}$, $I_{SINK}=0\text{mA}$, $T_A=25^{\circ}\text{C}$		-	2.1	3	

1.8 Thermal Characteristics

Parameter	Conditions	Symbol	Typ	Units
Thermal Impedance, Junction to Ambient	Free Air	$R_{\theta JA}$	114	°C/W
LED Temperature Coefficient	$I_F=1.5\text{mA}$	$\frac{dV_F}{dT}$	-1.3	mV/°C
Output Voltage Temperature Coefficient	$I_{SINK}=6\text{mA}$	$\frac{dV_{OUT}}{dT}$	1.2	mV/°C

1.9 Switching Specifications

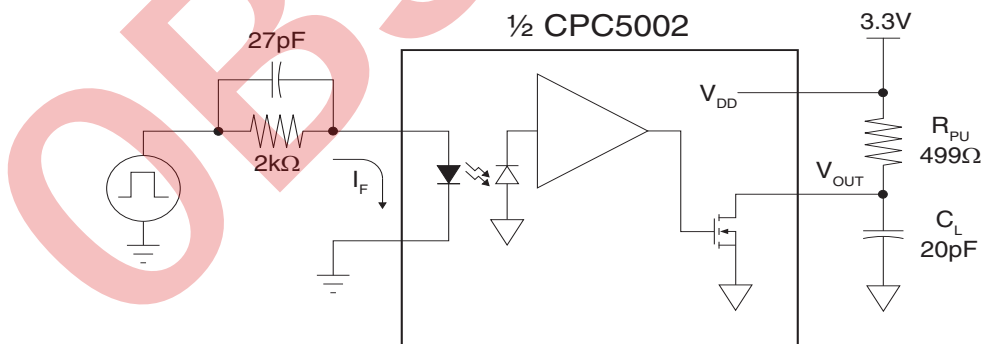
Parameter	Conditions	Symbol	Min	Typ	Max	Units
Timing Specifications						
Clock Frequency	$I_{SINK}=6mA, C_L=20pF$	f_{MAX}	-	10	-	MHz
Propagation Delay Output Falling ^{1,3} Output Rising ^{2,3}	$I_F=1.5mA, V_{DD}=3.3V,$ $R_{PU}=499\Omega, C_L=20pF,$ $0.5V_{IN}$ to $0.5V_{DD_OUT}$	t_{PHL}	35	81	120	ns
		t_{PLH}	35	81	120	
Pulse Width Distortion: $ t_{PLH} - t_{PHL} $	As per t_{PHL} and t_{PLH}	PWD	-	-	85	ns
Propagation Delay Skew ³	As per t_{PHL} and t_{PLH}	t_{PSK}	-	-	50	ns
Output Fall Time, 90% to 10%	$I_F=1.5mA, V_{DD}=3.3V,$ $R_{PU}=499\Omega, C_L=20pF$	t_f	10	15	-	ns
Common Mode Specifications						
Common Mode Transient Immunity	$V_{CM}=20V_{P-P}, V_{DD}=3.3V, T_A=25^\circ C$					
$V_{OUT} = \text{High}$	$V_{OUT} > 2V$	CM_H	5	-	-	kV/ μs
$V_{OUT} = \text{Low}$	$V_{OUT} < 0.8V$	CM_L	7	-	-	

¹ Falling propagation delay can be reduced by increasing instantaneous LED current drive, typically by increasing C_{FWD} .

² Rising propagation delay depends on R_{PU} , C_L , and I_F .
Increasing I_F above $2 \cdot I_{TH}$ (by reducing R_S) increases the rising propagation delay.

³ Propagation Delay Skew is the worst case difference propagation delay, High to Low and Low to High between the two channels of a CPC5002 when measured using the test circuit shown below, which is tuned for approximately even rising and falling delays.

1.10 Propagation Delay Test Circuit

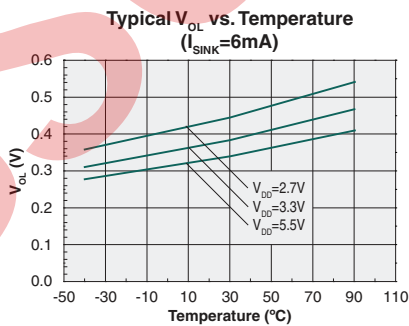
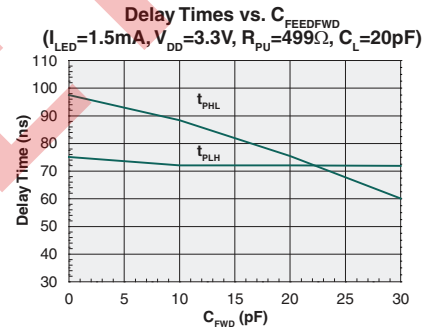
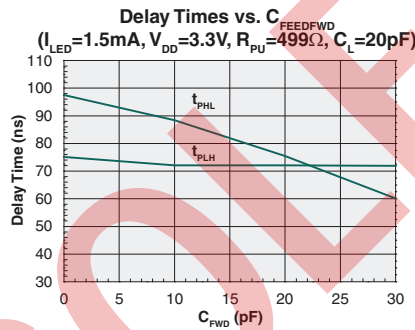
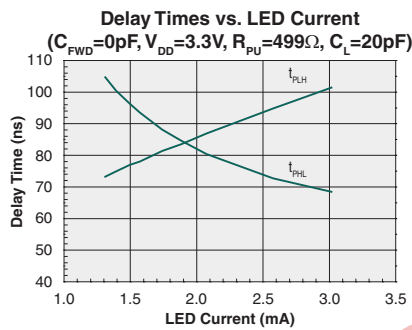
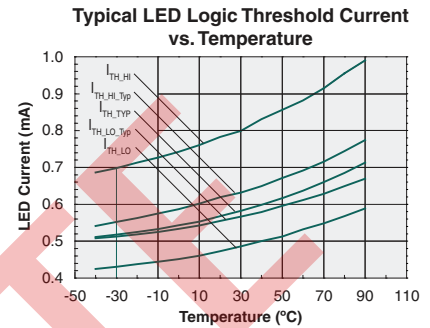
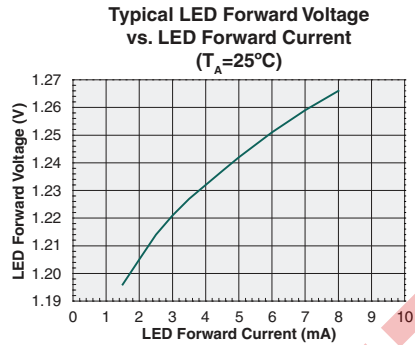
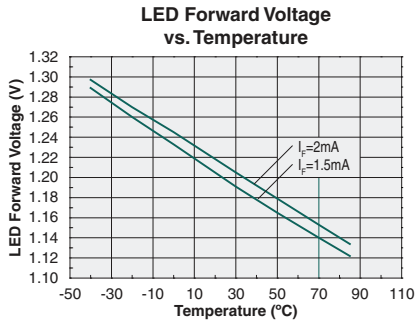


1.11 Typical Switching Waveforms

Typical @ $V_{DD} = 3.3V$, $I_F = 1.5mA$, $R_{PU} = 499\Omega$, $C_L = 20pF$
(Reference "Figure 2. Non-Inverting Configuration" on page 9)



2 Performance Data*



*Unless otherwise noted, data presented in these graphs is typical of device operation at 25°C. For guaranteed parameters not indicated in the written specifications, please contact our applications department.

3 Functional Description

3.1 Introduction

The CPC5002 provides two independent galvanically isolated high speed open-drain output optical isolators in a single 8-pin package. It exhibits excellent isolation (3750V_{rms}) and speed (10Mbps typical), and operates over a wide range of supply voltages (2.7V to 5.5V).

Because the active circuits have been fabricated in a CMOS process, the device requires much less supply current (1.4mA typical with V_{DD} = 3.3V) and can run at much lower LED currents (1.4mA minimum) than similar devices fabricated with bipolar processes.

3.2 Functional Description

An open-drain output of the CPC5002 will activate and sink current when the light generated by the LED and passed across the barrier to the photodetector is sufficient. The minimum level of input current necessary to initiate this behavior is referred to as the LED Input Threshold Current (I_{TH}) and is a function of the optical current transfer ratio of the device.

To provide consistent performance over the LED Input Threshold Current range, the recommended typical LED drive current (I_F) over temperature and all operating conditions, is 1.5mA. This recommendation is provided to offer a balance in the propagation delays on both the falling and rising edges of the signal pulse being buffered across the barrier. The absolute value of the mismatch in the delay of these two edges is Pulse Width Distortion. In the specifications these delays are identified as t_{PHL} and t_{PLH} while the distortion is PWD.

In general, choosing a higher LED drive current will decrease t_{PHL}, the propagation time for the output to go from high to low. This is mostly due to the LED generating more light more quickly as it turns on. However, if I_F is more than 2 x I_{TH} then increasing the LED drive current further will cause t_{PLH}, the propagation time for the output to go from low to high, to increase.

Excess levels of I_F makes the difference between t_{PLH} and t_{PHL} (also known as pulse width distortion) greater. Pulse width distortion is often of interest when the signal being isolated is a clock. Keeping the LED

drive current near 1.5mA and using the minimum R_{PU} and C_L at the output reduces the worst case pulse width distortion and is thus recommended for best waveform fidelity.

When using 1.5mA of LED drive current and when the CPC5002 is driving a fast output bus (one with minimum R_{PU} and C_L), the average t_{PHL} will usually be slightly longer than the average t_{PLH}. In this case, reduction of average pulse width distortion can be accomplished by using a small feed forward capacitor. The capacitor boosts the instantaneous current applied to the LED at turn-on (reducing t_{PHL}) while leaving the applied DC input current at 1.5mA (t_{PLH} unchanged). Examples of the feed forward capacitor (C_{FWD}) are shown in "Figure 1. Inverting Configuration" on page 9 and "Figure 2. Non-Inverting Configuration" on page 9. Increasing the value of the feed forward capacitor causes t_{PHL} to decrease. For a 499Ω pullup into a 20pF load capacitance (C_L), a 10pF capacitor across the series resistor will minimize pulse width distortion of an average unit.

When parallel digital signals are to be isolated, propagation delay skew (t_{PSK}) becomes important. It is defined as the absolute value of the difference between the maximum and minimum propagation delays (i.e. the worse of Δ t_{PLH} or Δ t_{PHL}) for any group of optical isolator channels operating under the same conditions. For the CPC5002, the delay t_{PLH} has a wider variation with differing optical current transfer ratios than the delay t_{PHL}. Additionally, t_{PLH} will exhibit variation due to R_{PU} and C_L differences between channels. If one channel is to be used as a clock and another for data, it is recommended to use the CPC5002 output falling edge to latch the data as this edge will exhibit less channel-to-channel or part-to-part timing variation and thus will reduce worst case timing skew.

In general the current transfer ratio matching between the two channels in a single CPC5002 is better than the ratio matching between multiple parts. Thus the channel to channel skew for two signals isolated through the same CPC5002 will be statistically better than skew measured between signals isolated through multiple parts.

3.3 Output Drivers

Designed specifically for data and clock busses, the output drivers have been configured for optimal performance and behavior.

To reduce RF emissions and ringing on the output lines the active low output drivers are slew limited. In addition to limiting emissions, the slew limited outputs reduce the need for external output series resistors.

Whenever the outputs are in the deasserted logic high state, the open-drain outputs exhibit low leakage performance while presenting a high impedance (Hi-Z) to the load. Additionally, during power-up and with the loss of V_{DD} , the outputs default to the Hi-Z deasserted state thereby ensuring signal integrity of any bussed, open-drain signals connected to the output pins

To maximize system design flexibility, the outputs are tolerant of pull-up voltages greater than the CPC5002 supply voltage, V_{DD} , provided the pull-up voltage remains within the output's specified voltage limits. For example, using a 3.3V supply to power the CPC5002, it's outputs may be safely operated into a pull up resistor to a supply voltage of 6.5V.

3.4 Power Supply Decoupling and Noise Reduction

There are no special power supply decoupling requirements for the CPC5002.

In addition, since the CPC5002 uses optical coupling to transfer information across the barrier, no internal clocking circuits are utilized to maintain the proper output state. This negates the need to implement the required special layout or noise reduction techniques necessary to maintain EMI or RFI compliance.

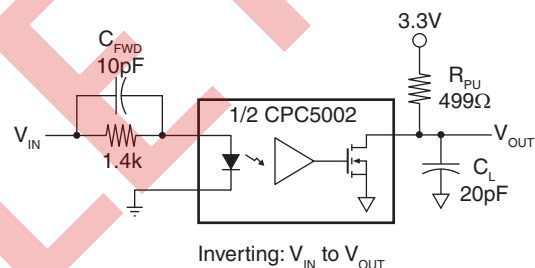
4 Circuit Examples

4.1 Inverting and Non-Inverting Configurations

Shown below are typical inverting and non-inverting circuit examples with the optional feed forward capacitors used for high speed signals.

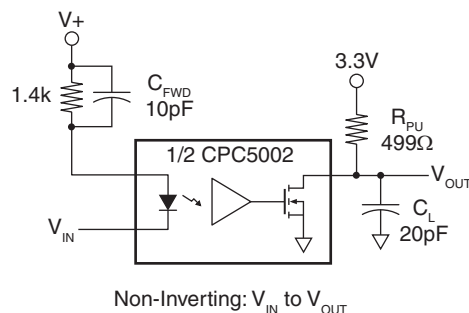
These designs assume a combined voltage drop of 3.3V across the input resistor and the LED with a nominal input current of 1.5mA.

Figure 1. Inverting Configuration



C_{FWD} increases instantaneous I_F at LED turn-on to reduce t_{PHL} at V_{OUT} .

Figure 2. Non-Inverting Configuration



For applications where the nominal total voltage drop across the input resistor and the LED is not 3.3V it will be necessary to adjust the input resistor's value. Examples of this would be different pull-up voltage supplies and V_{IN} sources that do not drive completely to the supply rails.

4.2 Application Example

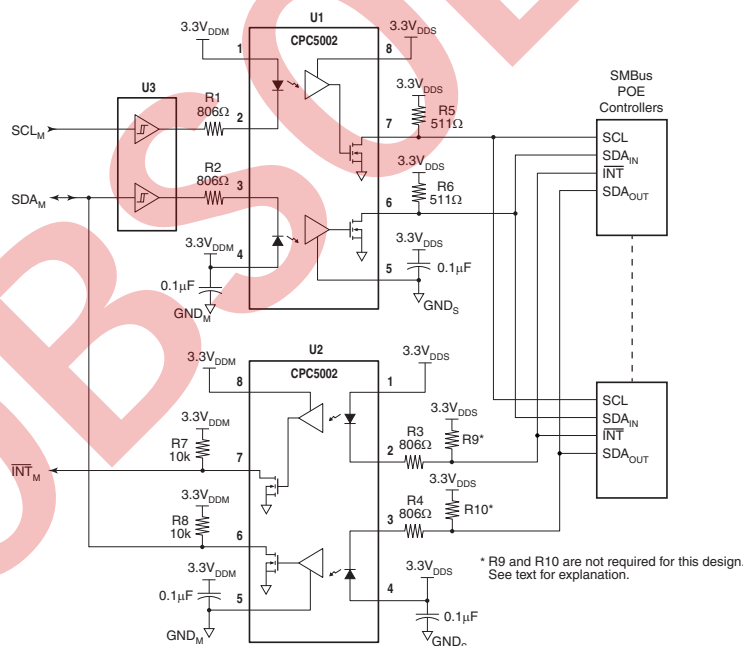
Shown below is an example of an isolated POE Controller SMBus where the SDA signal has been split into separate SDA_{IN} and SDA_{OUT} signals on the isolated slave side of the barrier. In this example, the low power SMBus master, not shown, requires a buffer (U3) capable of driving the CPC5002 input LEDs. Although selection of the appropriate buffer is determined by the product definition and the ability to drive the LED's, it is recommended the buffer have Schmitt trigger inputs to ensure clean bounce-free LED drive signals. A high power SMBus master with the ability to sink 4mA of pullup current may not require a buffer to drive the CPC5002 inputs. In this example, the POE Controllers are specified as SMBus high power and I^2C compatible. This enables the POE Controllers to drive the CPC5002 LEDs directly without the need of an external buffer.

Circuit design of the SMBus physical layer using the CPC5002 consists of two parts, one being the LED input drive current and the other being the buffered galvanically isolated logic output signals.

The following design constraints are assumed for this example:

- Supply Voltages: $V_{DDX} = 3.0V$ to $3.6V$
- Ambient Temperature: $T_A = 0^\circ C$ to $70^\circ C$
- $V_{OL} \leq 0.4V$ for U3 and the POE Controllers
- $I_{OL} \geq 4mA$ for U3 and the POE Controllers
- Resistors:
 - Tolerance = 1%
 - Temperature Coefficient = 100ppm

Figure 3. Optically isolated SMBus for POE Controllers with Separate SDA_{IN} and SDA_{OUT} Pins



To minimize pulse width distortion of the output signal, the input LED drive current needs to be set at the lower end of it's operational range. Because the forward voltage of the LED has a negative temperature coefficient this will occur at the minimum operating temperature point with the minimum supply voltage. With $V_{DD} = 3.0V$ and $V_F = 1.442V$ at $T_A = 0^\circ C$ and $I_F = 1.4mA$, the calculated maximum value for the series input resistor R_S is 826.8Ω . Taking tolerance and value change due to temperature into account, the nearest E96 standard value sets $R_S = 806\Omega$. Using $V_{OL_Nominal} = 0.25V$ and $V_{OL_Minimum} = 0.1V$ and calculating for the LED current range over the specified operating conditions with $R_S = 806\Omega$, the LED input current I_F will be $1.455mA$ to $3.212mA$. At nominal operating conditions with $T_A = 25^\circ C$, the nominal LED input current is: $I_{F_Nominal} = 2.28mA$.

For the outputs, the CPC5002 is compatible with both SMBus and Fast-mode I²C compatible devices. As with all mixed type devices on a bus, the weakest driver on that bus determines the minimum value of the pullup resistor. When the CPC5002 is the only device driving the bus as shown with U1, the minimum E96 standard value for pullup resistors R5 and R6 will be 511Ω. For bus loading up to 400pF, this pullup resistor value will provide for Fast-mode compliant I²C bus speeds. At lower data rates or with less capacitive bus loading, the actual resistor value selected can be higher.

When the CPC5002 shares a bus with another device as is the case with U2, the weakest driver sets the conditions for selecting the correct resistor value. As stated earlier, the SMBus master is rated as a Low-power device and therefore is only capable of sinking 350uA to an output low voltage level of 0.4V. A pullup resistor attached to the maximum supply voltage level of 3.6V and pulled down by this low power driver limits the minimum pullup resistor value to 9.14kΩ. After considering tolerance and temperature effects the nearest E96 standard value is 9.31kΩ. Most applications will typically select the more common 10kΩ value for R7 and R8, which allows for a 5% resistor tolerance.

Although shown but not needed in this example are pullup resistors R9 and R10. These resistors, not needed by the CPC5002 at U2, are utilized whenever the busses they are attached to are also connected to device(s) having logic level inputs. With heavy loading or excessive leakage on the bus the resistors provide supplementary bias to improve pullup transition performance and to increase the output logic high level without impacting the LED input current bias level.

The CPC5002 can be utilized to provide digital isolated buffering in a variety of unique applications. Design support is available by contacting IXYS Integrated Circuits' Applications Department.

5 Manufacturing Information

5.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
CPC5002GS	MSL 1

5.2 ESD Sensitivity



This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum total dwell time (t_p) in all reflow processes that the body temperature of these surface mount devices may be ($T_C - 5$)°C or greater. The device's body temperature must not exceed the Classification Temperature at any time during reflow soldering processes.

Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
CPC5002GS	250°C	30 seconds	3

For through-hole devices, the maximum pin temperature and maximum dwell time through all solder waves is provided in the table below. Dwell time is the interval beginning when the pins are initially immersed into the solder wave until they exit the solder wave. For multiple waves, the dwell time is from entering the first wave until exiting the last wave. During this time, pin temperatures must not exceed the maximum temperature given in the table below. Body temperature of the device must not exceed the limit shown in the table below at any time during the soldering process.

Device	Maximum Pin Temperature	Maximum Body Temperature	Maximum Dwell Time	Max Reflow Cycles
CPC5002G	260°C	250°C	10 seconds*	1

*Total cumulative duration of all waves.

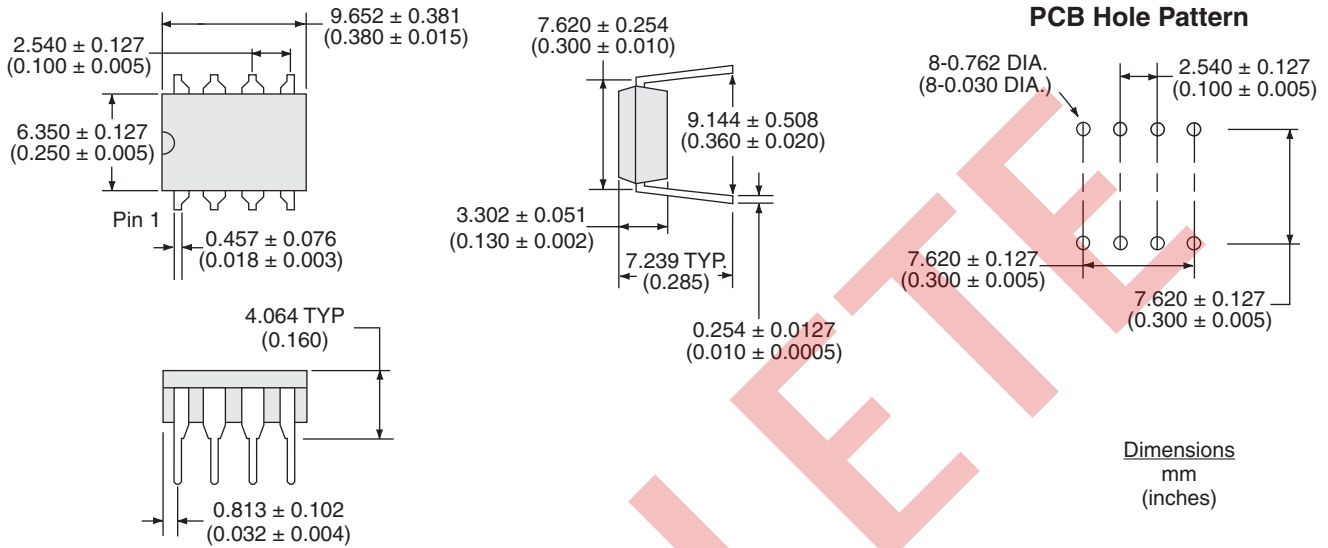
5.4 Board Wash

IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

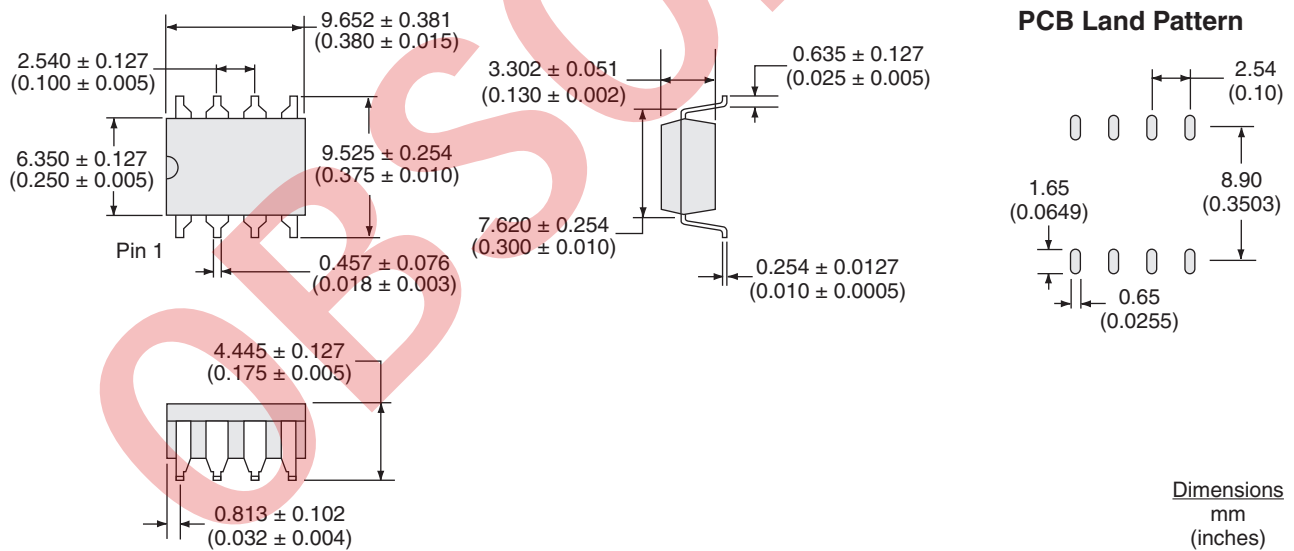


5.5 Mechanical Information

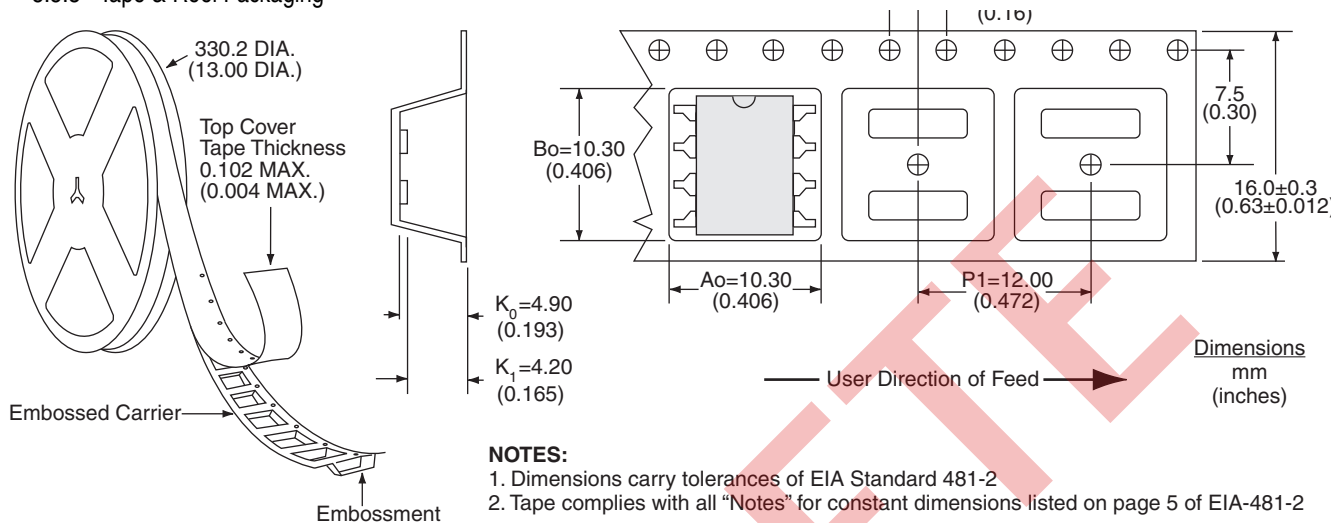
5.5.1 8-Pin DIP Package



5.5.2 8-Pin Surface Mount Package



5.5.3 Tape & Reel Packaging



For additional information please visit our website at: <https://www.ixysic.com>



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Specification: DS-CPC5002-ROBS
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