IXYS
INTEGRATED CIRCUITS DIVISION

CPC3909
400V, 6Ω N-Channel Depletion-Mode FET

Parameter	Rating	Units
Drain-to-Source Voltage - $V_{(BR)DSX}$	400	V
Max On-Resistance - $R_{DS(on)}$	6	Ω
Max Power		
SOT-89 Package	1.1	W
SOT-223 Package	2.5	W

Features
- 400V Drain-to-Source Voltage
- Depletion Mode Device Offers Low $R_{DS(on)}$ at Cold Temperatures
- Low On-Resistance: 4.5Ω (Typical) @ 25°C
- Low $V_{GS(off)}$ Voltage
- High Input Impedance
- Low Input and Output Leakage
- Small Package Size SOT-89 and SOT-223
- PC Card (PCMCIA) Compatible
- PCB Space and Cost Savings
- Flammability Rating UL 94 V-0

Applications
- LED Drive Circuits
- Telecommunications
- Normally On Switches
- Ignition Modules
- Converters
- Security
- Power Supplies
- Regulators

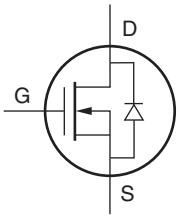
Description
The CPC3909 is an N-channel, depletion mode Field Effect Transistor (FET) that is available in an SOT-223 package (CPC3909Z) and an SOT-89 package (CPC3909C). Both utilize IXYS Integrated Circuits Division's proprietary vertical DMOS process that realizes world class, high voltage MOSFET performance in an economical silicon gate process. The vertical DMOS process yields a highly reliable device, particularly for use in difficult application environments such as telecommunications, security, and power supplies.

CPC3909Z and the CPC3909C have a typical on-resistance of 4.5Ω and a drain-to-source voltage of 400V. As with all MOS devices, the FET structure prevents thermal runaway and thermally induced secondary breakdown.

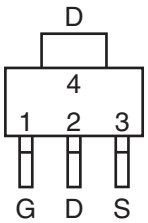
Ordering Information

Part Number	Description
CPC3909CTR	SOT-89: Tape and Reel (1000/Reel)
CPC3909ZTR	SOT-223: Tape and Reel (1000/Reel)

Circuit Symbol



Package Pinout:



Pin Number	Name
1	GATE
2	DRAIN
3	SOURCE
4	DRAIN

Pb RoHS e3

Absolute Maximum Ratings @ 25ºC

Parameter	Ratings	Units
Drain-to-Source Voltage ($V_{(BR)DSX}$)	400	V
Gate-to-Source Voltage (V_{GS})	15	V
Total Package Dissipation [1]		
SOT-89	1.1	W
SOT-223	2.5	W
Operational Temperature	-40 to +110	ºC
Storage Temperature	-40 to +125	ºC

[1] Mounted on 1"x1" FR4 board.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Typical values are characteristic of the device at +25°C, and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the manufacturing testing requirements.

Electrical Characteristics @25ºC (Unless Otherwise Specified)

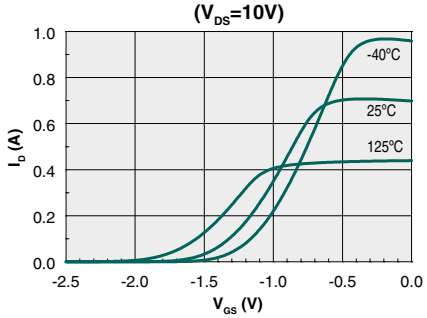
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Gate-to-Source Off Voltage	$V_{GS(off)}$	I_D=1µA, V_{DS}=5V	-1.4	-	-3.1	V
Drain-to-Source Leakage Current	$I_{DS(off)}$	V_{GS}= -5.5V, V_{DS}=240V	-	-	20	nA
		V_{GS}= -5.5V, V_{DS}=400V	-	-	1	µA
Drain Current	I_D	V_{GS}= 0V, V_{DS}=5V	300	-	-	mA
On-Resistance	$R_{DS(on)}$	V_{GS}= 0V, I_{DS}=300mA	-	4.5	6	Ω
Gate Leakage Current	I_{GSS}	V_{GS}=15V	-	-	100	nA
Gate Capacitance	C_{ISS}	V_{DS}= V_{GS}=0V	-	-	275	pF

Thermal Impedance

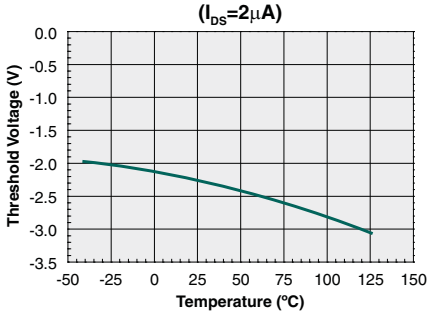
Device	Parameter	Symbol	Conditions	Min	Typ	Max	Units
SOT-89 (CPC3909C)	Junction to Case	θ_{JC}	-	-	-	50	ºC/W
	Junction to Ambient	θ_{JA}				90	
SOT-223 (CPC3909Z)	Junction to Case	θ_{JC}	-	-	-	14	
	Junction to Ambient	θ_{JA}				55	

PERFORMANCE DATA*

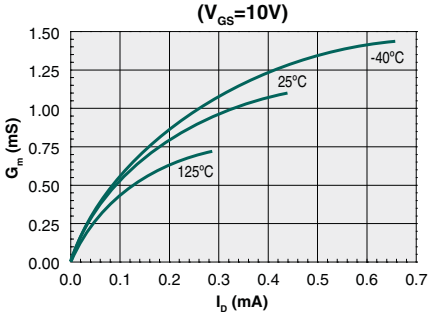
Instantaneous Transfer Characteristics (V_{DS}=10V)



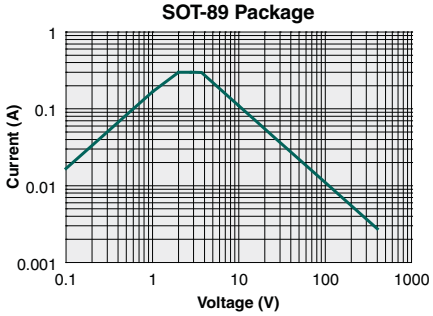
Threshold Voltage (I_{DS}=2μA)



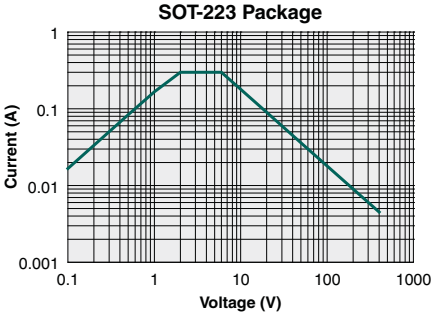
Transconductance vs. Drain Current (V_{GS}=10V)



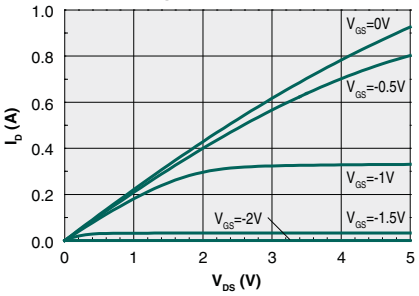
Forward Safe Operating Bias SOT-89 Package



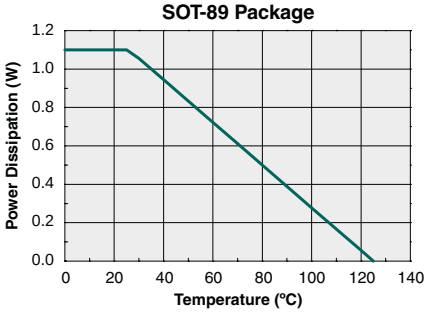
Forward Safe Operating Bias SOT-223 Package



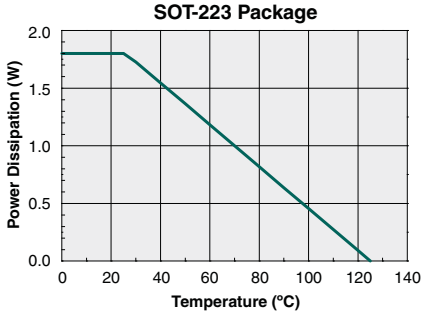
Output Characteristics



Power Dissipation vs. Ambient Temperature SOT-89 Package



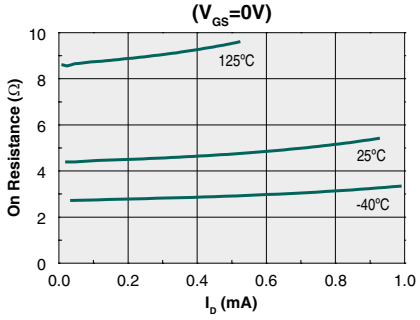
Power Dissipation vs. Ambient Temperature SOT-223 Package



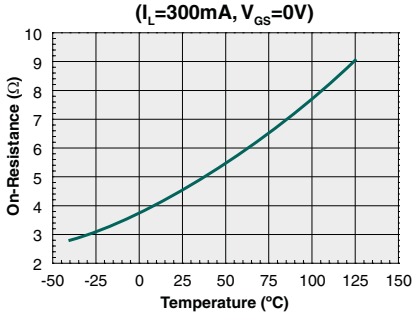
*Unless otherwise noted, data presented in these graphs is typical of device operation at 25°C.

PERFORMANCE DATA*

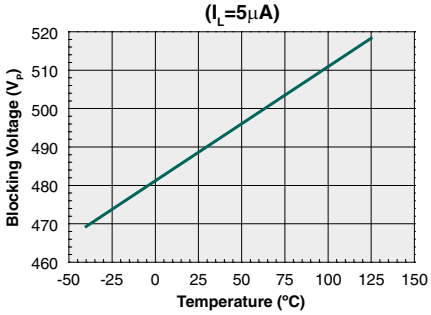
On-Resistance vs. Drain Current (V_{GS}=0V)



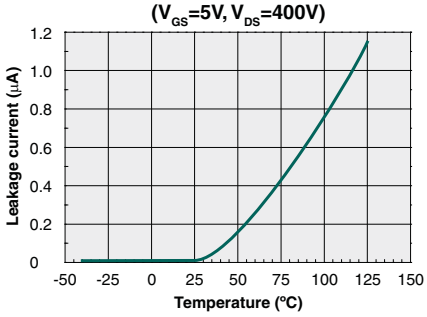
On-Resistance vs. Temperature (I_L=300mA, V_{GS}=0V)



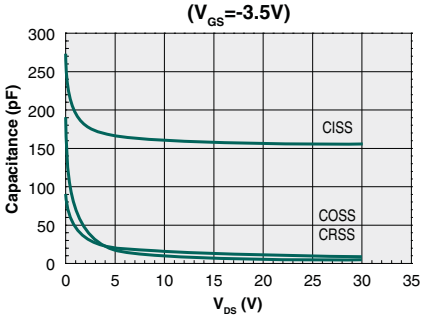
Blocking Voltage vs. Temperature (I_L=5μA)



Leakage Current vs. Temperature (V_{GS}=5V, V_{DS}=400V)



Capacitance vs. Drain-Source Voltage (V_{GS}=-3.5V)



*Unless otherwise noted, data presented in these graphs is typical of device operation at 25°C.

Manufacturing Information

Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
CPC3909C / CPC3909Z	MSL 1

ESD Sensitivity

This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum dwell time the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

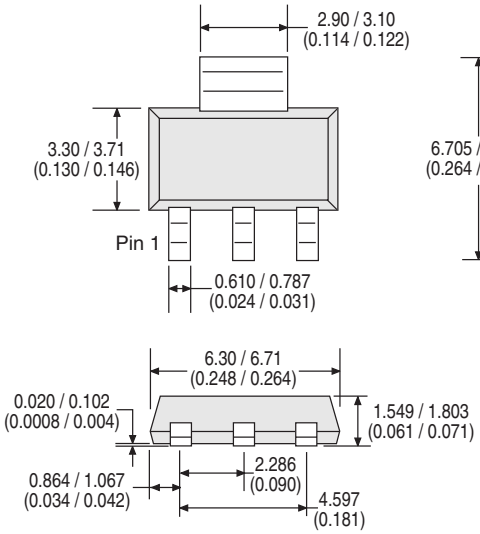
Device	Classification Temperature (T_c)	Dwell Time (t_p)	Max Reflow Cycles
CPC3909C / CPC3909Z	260°C	30 seconds	3

Board Wash

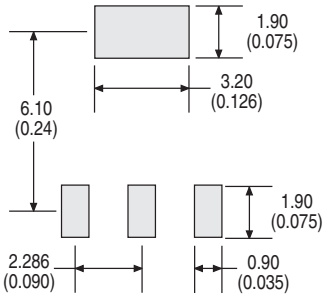
IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

MECHANICAL DIMENSIONS

CPC3909Z

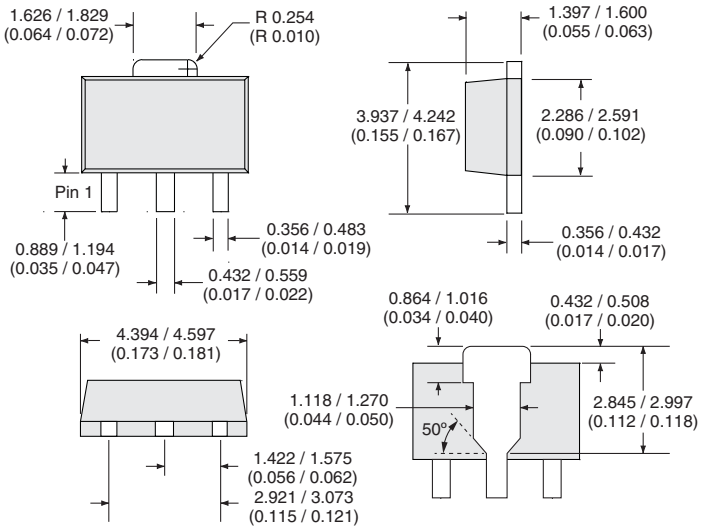


PCB Land Pattern

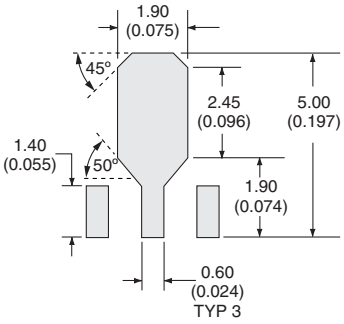


Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

CPC3909C



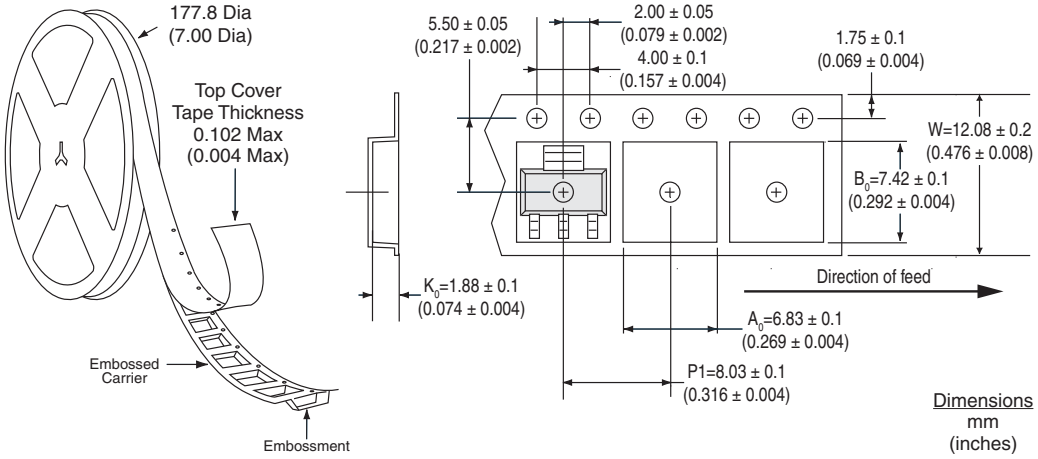
PCB Land Pattern



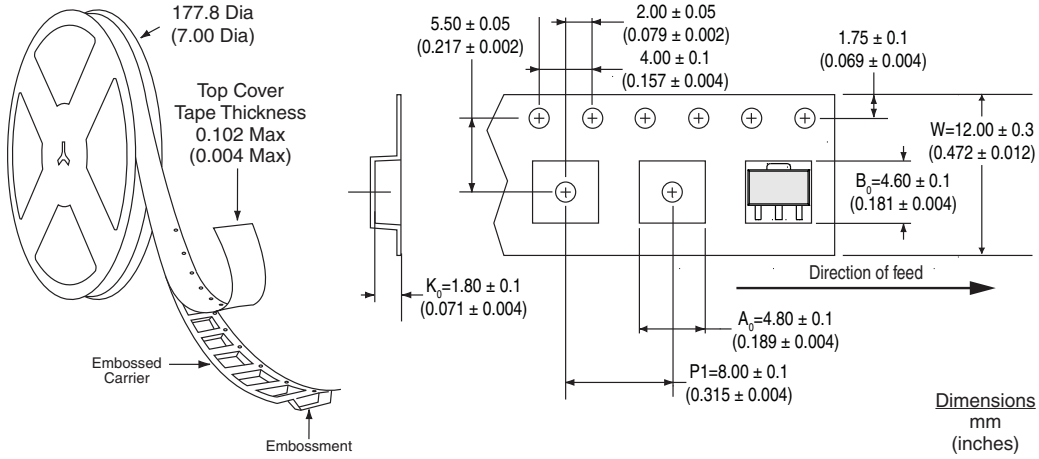
Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

MECHANICAL DIMENSIONS

CPC3909ZTR Tape & Reel



CPC3909CTR Tape & Reel



For additional information please visit our website at: www.ixysic.com

IXYS
A Littelfuse Technology

Specification: DS-CPC3909-R01

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