



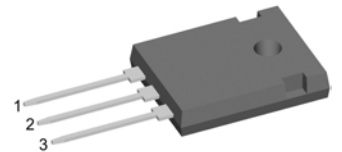
# High Efficiency Thyristor

$V_{RRM} = 1200\text{ V}$   
 $I_{TAV} = 40\text{ A}$   
 $V_T = 1,26\text{ V}$

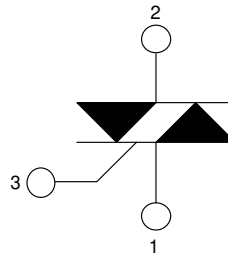
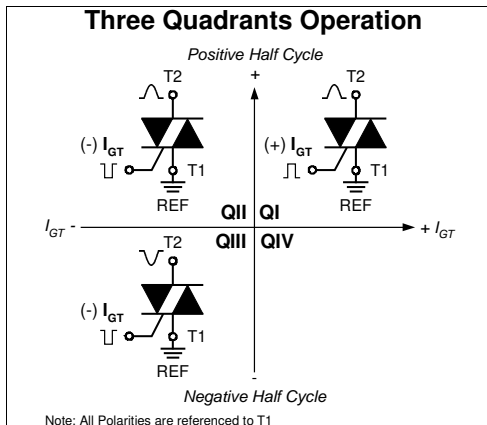
Three Quadrants operation: QI - QIII  
 1~ Triac

Part number

**CLA80MT1200NHR**



Backside: isolated



**Features / Advantages:**

- Triac for line frequency
- Three Quadrants Operation - QI - QIII
- Planar passivated chip
- Long-term stability of blocking currents and voltages

**Applications:**

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

**Package: ISO247**

- Isolation Voltage: 3600 V~
- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0
- Soldering pins for PCB mounting
- Backside: DCB ceramic
- Reduced weight
- Advanced power cycling

**Disclaimer Notice**

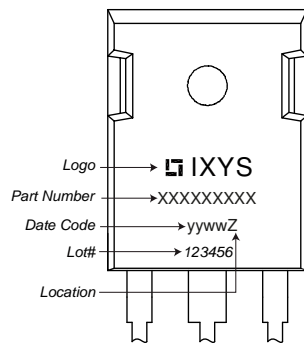
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Rectifier			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1200	V
$I_{RD}$	reverse current, drain current	$V_{R/D} = 1200 V$	$T_{VJ} = 25^{\circ}C$		10	$\mu A$
		$V_{R/D} = 1200 V$	$T_{VJ} = 125^{\circ}C$		2	mA
$V_T$	forward voltage drop	$I_T = 40 A$	$T_{VJ} = 25^{\circ}C$		1,30	V
		$I_T = 80 A$			1,59	V
		$I_T = 40 A$	$T_{VJ} = 125^{\circ}C$		1,26	V
		$I_T = 80 A$			1,64	V
$I_{TAV}$	average forward current	$T_C = 100^{\circ}C$	$T_{VJ} = 150^{\circ}C$		40	A
$I_{RMS}$	RMS forward current per phase	180° sine			88	A
$V_{T0}$	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}C$		0,88	V
$r_T$	slope resistance				10	m $\Omega$
$R_{thJC}$	thermal resistance junction to case				0,65	K/W
$R_{thCH}$	thermal resistance case to heatsink			0,25		K/W
$P_{tot}$	total power dissipation		$T_C = 25^{\circ}C$		190	W
$I_{TSM}$	max. forward surge current	$t = 10 ms$ ; (50 Hz), sine	$T_{VJ} = 45^{\circ}C$		520	A
		$t = 8,3 ms$ ; (60 Hz), sine	$V_R = 0 V$		560	A
		$t = 10 ms$ ; (50 Hz), sine	$T_{VJ} = 150^{\circ}C$		440	A
		$t = 8,3 ms$ ; (60 Hz), sine	$V_R = 0 V$		475	A
$I^2t$	value for fusing	$t = 10 ms$ ; (50 Hz), sine	$T_{VJ} = 45^{\circ}C$		1,35	kA <sup>2</sup> s
		$t = 8,3 ms$ ; (60 Hz), sine	$V_R = 0 V$		1,31	kA <sup>2</sup> s
		$t = 10 ms$ ; (50 Hz), sine	$T_{VJ} = 150^{\circ}C$		970	A <sup>2</sup> s
		$t = 8,3 ms$ ; (60 Hz), sine	$V_R = 0 V$		940	A <sup>2</sup> s
$C_J$	junction capacitance	$V_R = 400V$ $f = 1 MHz$	$T_{VJ} = 25^{\circ}C$		25	pF
$P_{GM}$	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 150^{\circ}C$		10	W
		$t_p = 300 \mu s$			5	W
$P_{GAV}$	average gate power dissipation				0,5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 150^{\circ}C$ ; $f = 50 Hz$ repetitive, $I_T = 120 A$			150	A/ $\mu s$
		$t_p = 200 \mu s$ ; $di_G/dt = 0,3 A/\mu s$ ; $I_G = 0,3A$ ; $V_D = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 40 A$			500	A/ $\mu s$
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V_D = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty$ ; method 1 (linear voltage rise)	$T_{VJ} = 150^{\circ}C$		500	V/ $\mu s$
$V_{GT}$	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1,7	V
			$T_{VJ} = -40^{\circ}C$		1,9	V
$I_{GT}$	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		$\pm 70$	mA
			$T_{VJ} = -40^{\circ}C$		$\pm 90$	mA
$V_{GD}$	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}C$		0,2	V
$I_{GD}$	gate non-trigger current				$\pm 1$	mA
$I_L$	latching current	$t_p = 10 \mu s$	$T_{VJ} = 25^{\circ}C$		100	mA
		$I_G = 0,3A$ ; $di_G/dt = 0,3 A/\mu s$				
$I_H$	holding current	$V_D = 6 V$ $R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		70	mA
$t_{gd}$	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	$\mu s$
		$I_G = 0,3A$ ; $di_G/dt = 0,3 A/\mu s$				
$t_q$	turn-off time	$V_R = 100 V$ ; $I_T = 40A$ ; $V_D = \frac{2}{3} V_{DRM}$ $di/dt = 10 A/\mu s$ ; $dv/dt = 20 V/\mu s$ ; $t_p = 200 \mu s$	$T_{VJ} = 125^{\circ}C$		150	$\mu s$

Package ISO247		Ratings				
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$I_{RMS}$	RMS current	per terminal			70	A
$T_{VJ}$	virtual junction temperature		-55		150	°C
$T_{op}$	operation temperature		-55		125	°C
$T_{stg}$	storage temperature		-55		150	°C
<b>Weight</b>				6		g
$M_D$	mounting torque		0,8		1,2	Nm
$F_C$	mounting force with clip		20		120	N
$d_{Spp/App}$	creepage distance on surface   striking distance through air	terminal to terminal	2,7			mm
$d_{Spb/Apb}$		terminal to backside	4,1			mm
$V_{ISOL}$	isolation voltage	t = 1 second	3600			V
		t = 1 minute	3000			V

### Product Marking



### Part description

C = Thyristor (SCR)  
 L = High Efficiency Thyristor  
 A = (up to 1200V)  
 80 = Current Rating [A]  
 MT = 1~ Triac  
 1200 = Reverse Voltage [V]  
 N = Three Quadrants operation: QI - QIII  
 HR = ISO247 (3)

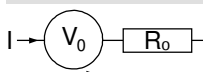
Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA80MT1200NHR	CLA80MT1200NHR	Tube	30	517123

Similar Part	Package	Voltage class
CLA40MT1200NHR	ISO247 (3)	1200
CLA60MT1200NHR	ISO247 (3)	1200
CLA80MT1200NHB	TO-247AD (3)	1200

### Equivalent Circuits for Simulation

\* on die level

$T_{VJ} = 150^{\circ}\text{C}$

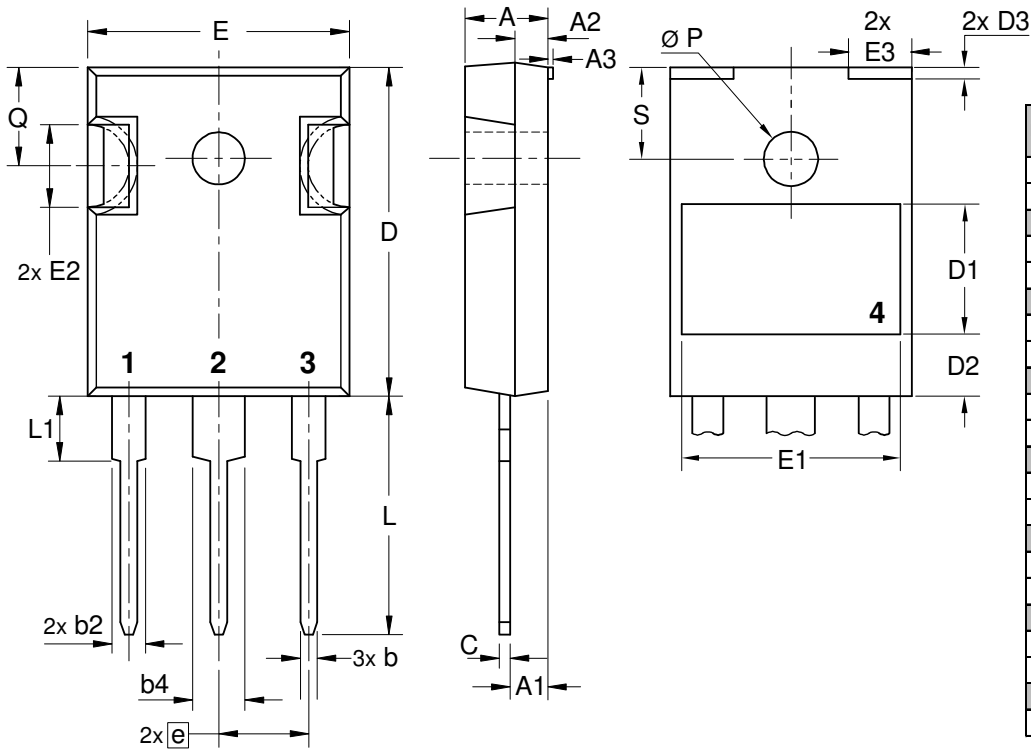


Thyristor

$V_{0 \max}$	threshold voltage	0,88	V
$R_{0 \max}$	slope resistance *	7,5	mΩ



Outlines ISO247



Dim.	Millimeter		Inches	
	min	max	min	max
A	4.70	5.30	0.185	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
A3	typ. 0.05		typ. 0.002	
b	0.99	1.40	0.039	0.055
b2	1.65	2.39	0.065	0.094
b4	2.59	3.43	0.102	0.135
c	0.38	0.89	0.015	0.035
D	20.79	21.45	0.819	0.844
D1	typ. 8.90		typ. 0.350	
D2	typ. 2.90		typ. 0.114	
D3	typ. 1.00		typ. 0.039	
E	15.49	16.24	0.610	0.639
E1	typ. 13.45		typ. 0.530	
E2	4.31	5.48	0.170	0.216
E3	typ. 4.00		typ. 0.157	
e	5.46 BSC		0.215 BSC	
L	19.80	20.30	0.780	0.799
L1	-	4.49	-	0.177
Ø P	3.55	3.65	0.140	0.144
Q	5.38	6.19	0.212	0.244
S	6.14 BSC		0.242 BSC	



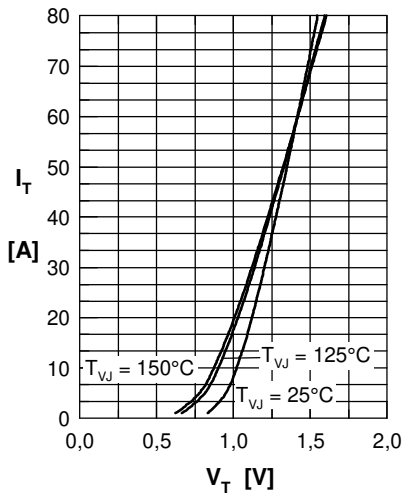
**Thyristor**


Fig. 1 Forward characteristics

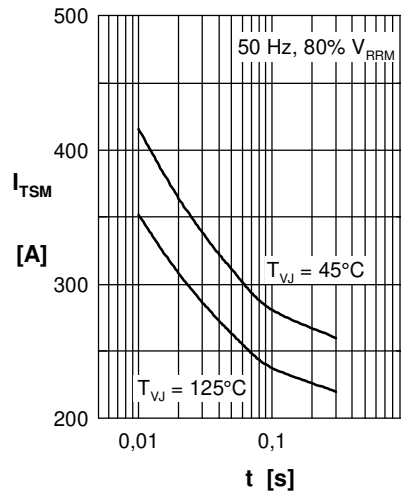
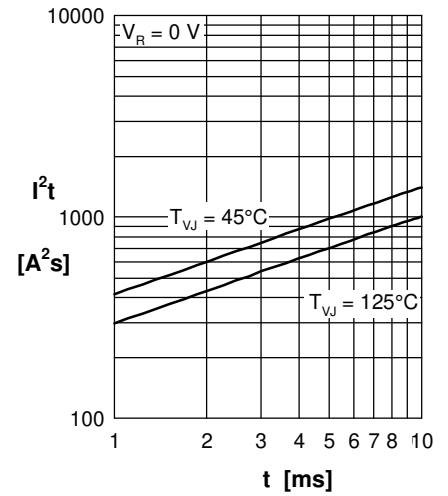
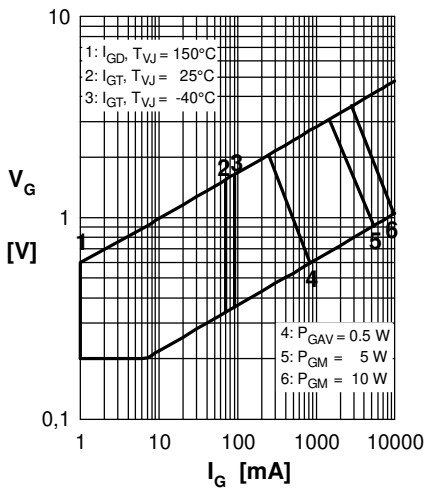

 Fig. 2 Surge overload current  
 $I_{TSM}$ : crest value,  $t$ : duration

 Fig. 3  $I^2t$  versus time (1-10 s)


Fig. 4 Gate voltage &amp; gate current

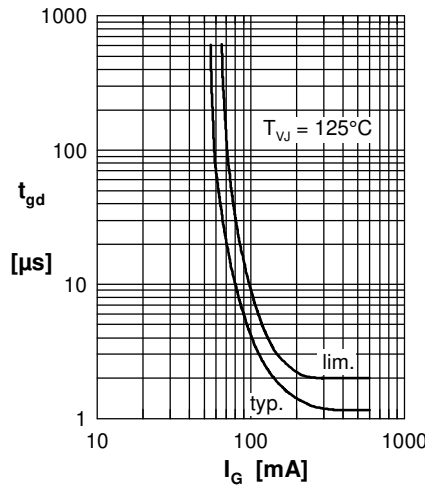
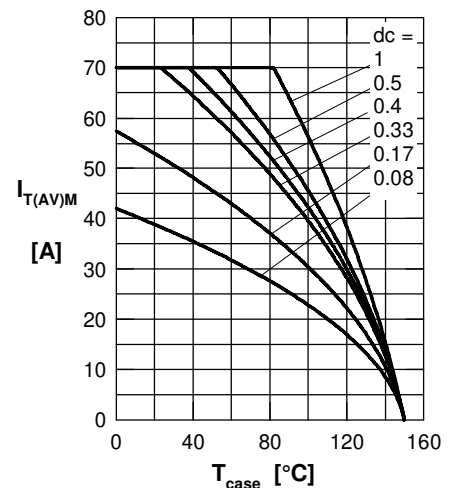

 Fig. 5 Gate controlled delay time  $t_{gd}$ 


Fig. 6 Max. forward current at case temperature

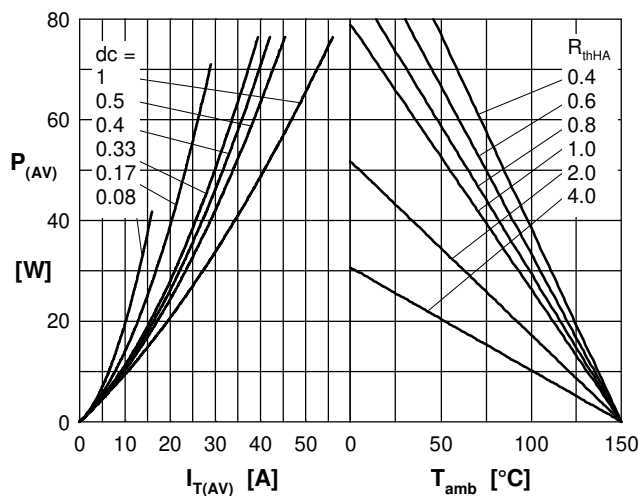
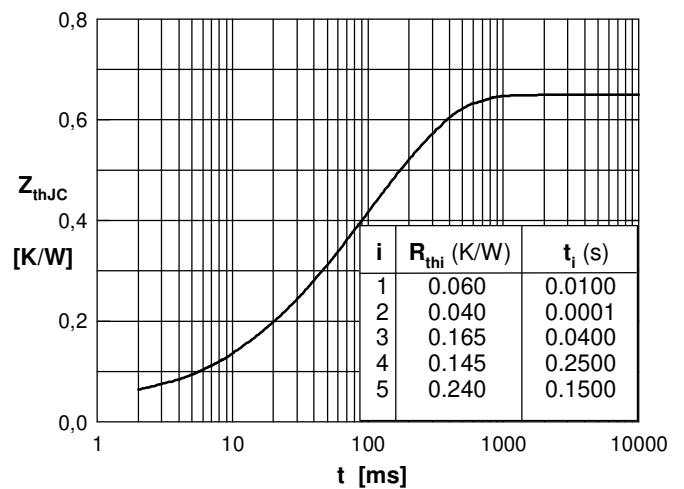

 Fig. 7a Power dissipation versus direct output current  
 Fig. 7b and ambient temperature


Fig. 7 Transient thermal impedance junction to case