Silicon-based 3-level T-type Neutral Boost Rectifier Integrated into SMPD Package

Abstract

Public DC-charging infrastructure is connected to the public three-phase low-voltage grid. Therefore, it must comply with the corresponding grid codes. The widely adopted Vienna Rectifier variants allow fulfilling this requirement and offer very high efficiency at low circuit complexity. The 3-level T-type neutral boost rectifier, also known as the original Vienna Rectifier, allows the use of fast 650 V Silicon-switches and fast 1200 V diodes. This paper evaluates a methodology to integrate the 3-level T-Type neutral boost rectifier into a compact Surface Mounted Power Device (SMPD) package and the power– and efficiency levels that can be achieved with different diode types.

Applications

- DC-charging stations
- Switched-mode power supplies

Target Audience

This document is intended for design engineers of power electronics for EV DC-charging stations or other power supplies.

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Introduction

Current electric vehicle (EV) DC-chargers at power levels between 250 kW and 350 kW are often built in a modular manner based on power subunits of 60-80 kW output power each [1,2]. This approach is well-known in the design of server power supplies in data centers, which comply with requirements for high efficiency, high reliability, and simple maintainability. **Figure 1** illustrates a block diagram of such a power sub-unit.

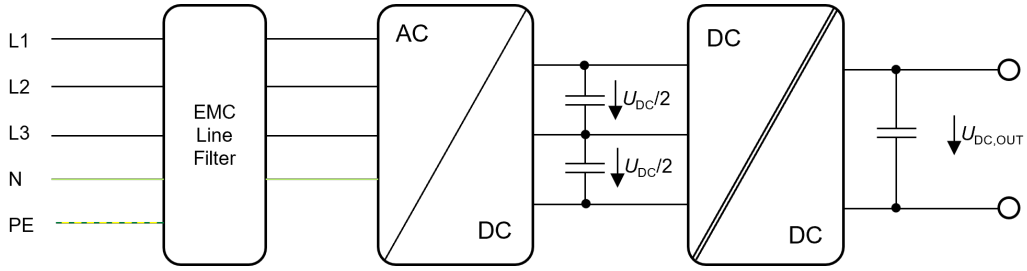


Figure 1. Block Diagram of a Power Supply Unit of a DC-charger

The power electronics inside the AC-DC subcircuit convert the line voltages into DC-voltage and form the input current to sinusoidal waveforms, in addition to performing a power factor correction (PFC) to control the phase-angle φ between line voltage and currents. Common approaches include, but are not limited to:

- Parallel connection of three single-phase power-stages, for example, bridge rectifier plus boost converter or totem pole PFC stages,
- A three-phase active full-bridge [3], or
- A Vienna-based topology, for example, symmetric boost PFC or 3-level T-Type neutral boost PFC

The first approach is not the best suitable option for DC-chargers of the targeted power levels, primarily because it requires a higher number of design variants to be compatible with grid connections with and without present neutral wire, as well as a very high number of rectifier diodes. When utilizing a three-phase active full-bridge, a lower efficiency and higher filtering efforts are evident when using 1200 V Silicon (Si) Insulated Gate Bipolar Transistors (IGBT). On the other hand, high efficiency but high-cost results are observed when using Silicon Carbide (SiC) Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs). However, if bi-directional power flow is required, this approach is well suited. In contrast to this, using a Vienna-based topology offers low cost at high efficiency and reduced filtering efforts when using Si devices such as 650 V Power MOSFETs or fast 650 V IGBTs in conjunction with fast recovery diodes (FREDs).

1. The 3-Level T-Type Neutral Boost PFC

The 3-Level T-Type neutral boost PFC is based on the Vienna Rectifier. **Figure 2** depicts the circuit diagram of the 3-Level T-type neutral boost PFC.

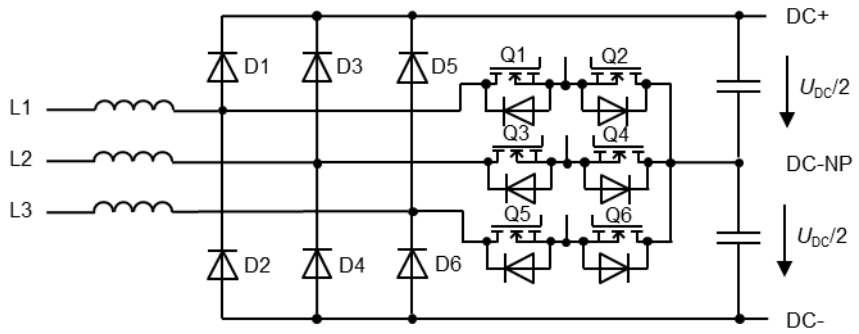


Figure 2. Circuit Diagram of the 3-level T-type Neutral Boost PFC

Basically, it functions as a boost converter with reference to the neutral or mid-point of the DC-link. Thus, it can operate in boost-mode during positive and negative half-waves of the grid's input voltage like a single-phase PFC stage. The diodes D1 to D6 need to block the full DC-link voltage U_{DC} and need to be rated for a blocking voltage of 1200 V. Therefore, to achieve high efficiency at high switching speeds, Si FREDs or SiC Schottky barrier diodes (SBD) are often used. Alternatively, series-connected 600 V Si FREDs, known as HiPerDynFREDs, can be used, as shown in **Figure 3.**

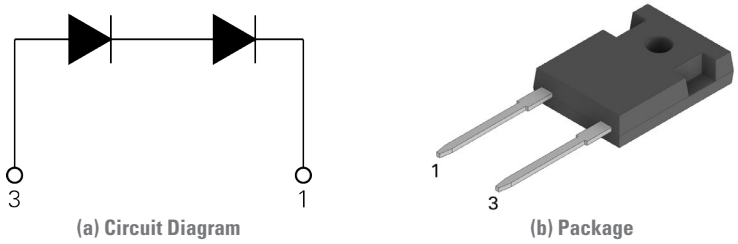


Figure 3. HiPerDynFRED in Discrete TO-247 Package [5]

The boost switches Q1 to Q6 only need to block half the DC-link voltage $U_{DC}/2$, which allows for utilizing 650 V MOSFETs.

To achieve the effect of PFC, the input current is formed sinusoidal by boosting the DC-link voltage to a higher voltage than the rectified line voltage. Values of U_{DC} = 750 V from $\hat{u}$ = 565 V are common. The switch then needs to block $U_{DC}/2$ = 375 V. With a margin of 25%, a MOSFET with a breakdown voltage of $U_{DS,max} \geq$ 500 V would be suitable. Consequently, a 650 V device is suitable for DC-link voltages up to $U_{DC} \leq$ 975 V. To achieve the output voltage required by the DC EV charging standard IEC61851-23 either a transformer with a ratio ≥ 1 in the DC-DC subcircuit or boosting the DC-link voltage to suitable levels can be considered. The DC-DC stage can be designed by using a phase-shifted full-bridge or other resonant switching converters, such as the LLC-topology. When the AC-DC circuit provides a split DC-link voltage, as given here, the outputs of two separate DC-DC stages are series-connected. Thus, 650 V switches can be used again to achieve high efficiency at lower cost.

2. Surface Mounted Power Device (SMPD) Package

To reduce assembly cost, surface mounted devices (SMD) are advantageous compared to discrete devices in through-hole technology. Additionally, power modules with direct-copper bonded (DCB) ceramic insulation ease thermal management, enhance assembly capabilities, and enable integrating suitable circuits with smaller loop inductance. The SMPD package combines the advantages of Integrated Power Modules (IPMs) with those of SMDs including the possibility to distribute thermal heat dissipation.

Figure 4 contains a rendering of the SMPD package.

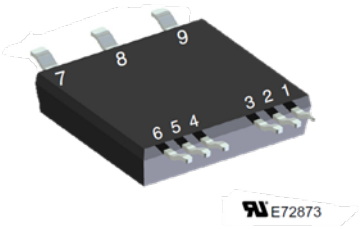


Figure 4. Model of the Surface Mounted Power Device (SMPD) Package, here as Variant B with Three Main Terminals 7-9 and Six Auxiliary Terminals 1-6

The device is a molded package with a DCB ceramic soldered to a lead-frame. It covers a PCB footprint of 25×32.7 mm² and has a height of 5.5 mm. The low weight of approximately 8.5 grams allows automatic assembly. The total DCB area is 21×23 mm² = 483 mm². Due to the lead-frame, an area of approximately 330 mm² is available for die placing and bonding. Additionally, the lead-frame provides a limited number of pins. The main terminals 7 to 9 can handle currents up to 100 A and terminals 1 to 6 up to 50 A, each.

3. Fitting the 3-Level T-Type neutral boost PFC into the SMPD

The 3-Level T-Type neutral boost PFC requires four power path terminals and three gate drive terminals. To fit one phase-leg into this package, the MOSFETs need to be mounted common-source. **Figure 5** illustrates the internal circuit and resulting terminal configuration, with optimized commutation loop. As the common-source configuration allows controlling both MOSFETs with the same gate-drive voltage, only 3 control-pins are required.

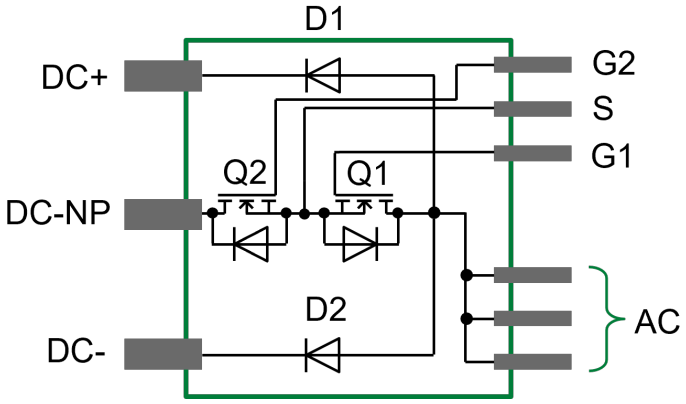
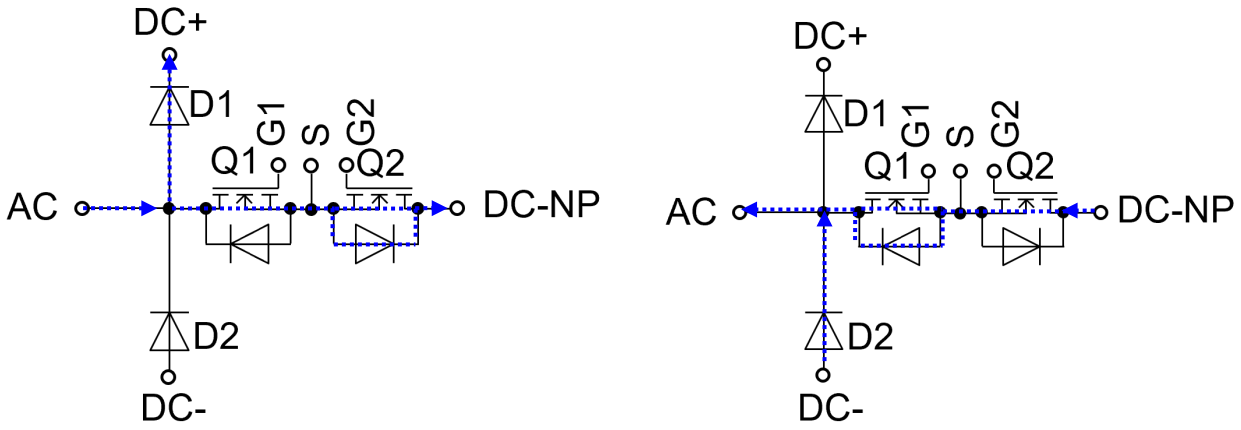


Figure 5. Circuit Schematic of the 3-Level T-Type Neutral Boost Phase-leg in the SMPD Footprint

Therefore, three small auxiliary pins can be used as the common AC-terminal, as indicated in **Figure 5** on the right.

The current paths within one phase-leg during positive and negative half-wave of the AC grid-voltage are depicted in **Figure 6 (a)** and **Figure 6 (b)**. They are identical to the classical boost converter cell. Depending on the control signals, the body diode or the MOSFET channel can conduct the freewheeling current.



(a) Positive half-wave of the AC grid voltage **(b) Negative half-wave of the AC grid voltage**

Figure 6. Illustration of Current Paths during both Half-waves of the AC Grid Voltage

Due to the limited SMPD DCB area, a 73 mΩ Si MOSFET chip with an active chip area of ~38 mm² is the largest possible option. Soldered onto an Al_2O_3 DCB, it achieves an approximate thermal resistance of R_{thJC} = 0.5 K/W, which results in a maximum DC-current of $I_{D,max}$ = 34 A at a junction temperature of T_{vj} = 150°C and the defined heatsink temperature of T_{HS} = 60°C. **Table 1** lists the considered operating parameters.

Table 1. Operating Parameters for Semiconductor Loss Calculations

Parameters	Description	Value
U_{AC}	Line Voltage	400 V
I_{AC}	Input Current	32 A
U_{DC}	DC-link Voltage	750 V
f_{SW}	Switching Frequency	48 kHz
T_{HS}	Heatsink Temperature	60°C

4. Measurement Setup

To evaluate whether the targeted SMPD integration is feasible, the semiconductor losses of different MOSFET-Diode combinations were measured using double pulse testing of discrete devices.

For this purpose, a Littelfuse-own characterization setup was used; see **Figure 7**.

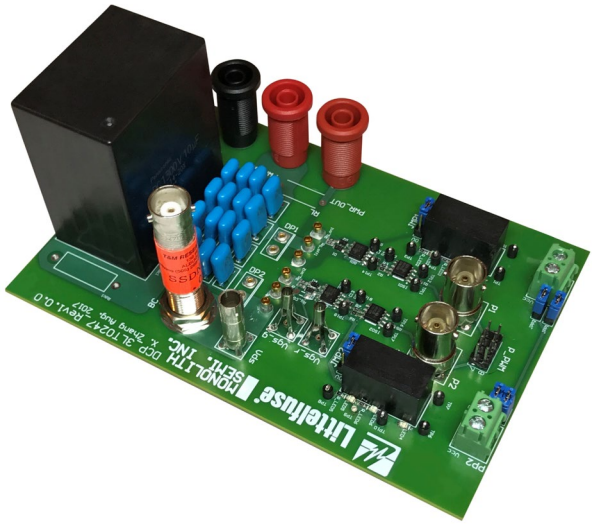


Figure 7. Littelfuse Dynamic Characterization Platform [4]

The applied gate drive voltages are $U_{GS,off}$ = −5 V and $U_{GS,on}$ = +15 V. An external gate resistance of $R_{G,ext}$ = 30 Ω was utilized for comparison. The drain current is sensed using a coaxial shunt of R_{sense} = 10.28 mΩ. Drain-Source voltage U_{DS} and Gate-Source voltage U_{GS} of the Device under test (DUT) were measured using PMK 1:1000 and PP026 1:10 passive probes, respectively.

Table 2 lists the MOSFET and diodes tested in double pulse characterization.

Table 2. Overview of Littelfuse MOSFET and Diodes for Double-pulse Testing [5-9]

DUT	Type	Parameters
IXFH46N65X3	Ultrajunction MOSFET	650 V, 73 mΩ, 46 A
DSEP12-12A	HiPerFRED	1200 V, 12 A
DSEP30-12B	HiPerFRED	1200 V, 30 A
DSEP15-12CR	HiPerDynFRED	1200 V, 15 A
LSIC2SD120A10	SiC Schottky	1200 V, 10 A

For comparison, the switching losses for each MOSFET-Diode combination were measured for Drain-currents 10 A ≤ I_D ≤ 50 A at a DC-voltage of U_{DC} = 400 V and at T_{vj} = 25°C.

5. Measurement Results

The switching loss energies extracted from double pulse testing of the different DUT combinations listed in **Table 2** are illustrated in **Figure 8**.

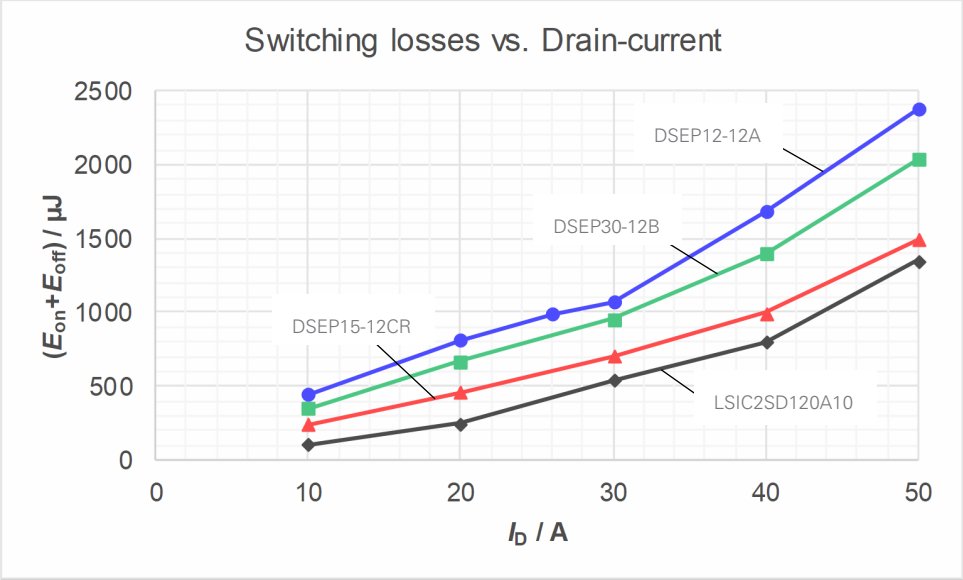


Figure 8. Total Switching Loss Energies of tested 1200 V Si FREDs and SiC Schottky Diode with the Ultrajunction MOSFET IXFH46N65X3 at DC-voltage of U_{DC} = 400 V

From the results, it can be seen that the use of the HiPerDynFRED DSEP15-12CR, with two series-connected 600 V Si FREDs, can improve the switching losses significantly compared to the 1200 V soft HiPerFRED DSEP12-12A. Due to the series connection of the 600 V Si FREDs, the total reverse recovery charge is very low. A compromise between both diodes is the optimized 1200 V HiPerFRED DSEP30-12B. It is a bigger die but has shorter reverse recovery time t_{rr} than the DSEP12-12A diode. As the measurements were conducted at low junction temperature of T_{vj} = 25°C, the losses at high junction temperature need to be considered carefully in system design. The SiC Schottky Barrier Diode (SBD) LSIC2SD120A10 has a nominal forward current of I_f = 15 A at a case temperature of T_C = 125°C [9] and thus would be the alternative chip. The switching losses of the SiC SBD are lower by about 43% compared to the DSEP12-12A at 50 A. Compared to the HiPerDynFRED, the SiC SBD reduces the switching losses by 9.6% at 50 A.

6. Application-specific Design

From the measured switching losses (E_{on}+E_{off}) given in **Figure 8** and the known on-resistance $R_{DS,on}$ of the MOSFET, as well as the forward voltage drop U_F of the diodes, the semiconductor losses of the 3-Level T-type neutral boost PFC phase-leg can be estimated with regard to the operating conditions summarized in **Table 1**.

To do so, the grid input current can be assumed sinusoidal at the given value of I_{AC} = 32 A. Using the targeted switching frequency of f_{sw} = 48 kHz, the average current value of each switching period can be calculated. Thus, the switching losses can be linearized from the graph of the measured results as regression functions, shown in **equations 1** to **4**:

$$\text{DSEP12-12A: } E(i) = 326.15e^{(0.0406 \cdot i)}\mu J \quad (1)$$

$$\text{DSEP30-12B: } E(i) = 254.3e^{(0.0426 \cdot i)}\mu J \quad (2)$$

$$\text{DSEP15-12CR: } E(i) = 175.22e^{(0.0438 \cdot i)}\mu J \quad (3)$$

$$\text{LSIC2SD120A10: } E(i) = 65.914e^{(0.0627 \cdot i)}\mu J \quad (4)$$

Since the working principles of the 3-Level T-type and the boost converter are the same, the losses can be calculated for one half-period of the grid frequency and applied throughout the complete cycle to each device. This means that the duty cycle can be calculated according to **equation 5**:

$$D(t) = 1\text{-}u(t)/(U_{DC}/2) \quad (5)$$

Figure 10 illustrates the calculated duty cycle for each switching period for an input voltage of $U_{AC,rms}$ = 400 V and a DC-link voltage of U_{DC} = 750 V and input current of I_{AC} = 32 A.

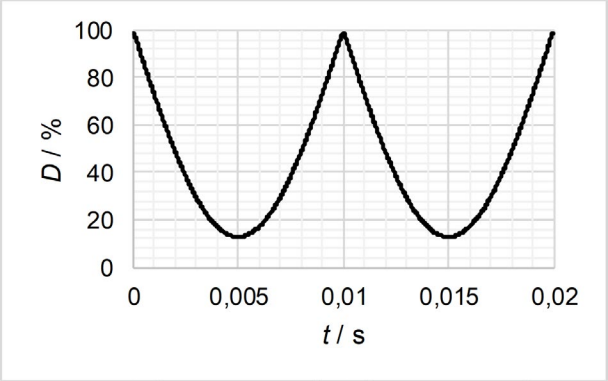


Figure 9. Duty Cycle as a Function of Time

By segmenting the sinusoidal input current and using the duty cycle from **Figure 9**, the average currents of the affected diode and MOSFET per cycle and thus, the switching losses according to **equations 1** to **4** can be calculated. The conduction losses are calculated using the average currents.

Table 3 lists the calculated switching and conduction losses of the possible MOSFET and Diode combinations at T_{vj} = 25°C.

Table 3. Calculated Semiconductor Losses of tested MOSFET IXFH46N65X3 and Different Diodes in 3-Level T-Type Neutral Boost PFC at T_{vj} = 25°C

@T_J = 25°C	DSEP12-12A	DSEP30-12B	DSEP15-12CR	LSIC2SD120A10
$P_{SW,MOS}$	14.6 W	12.2 W	8.8 W	6.6 W
$P_{cond,MOS}$	19.4 W	19.4 W	19.4 W	19.4 W
$P_{cond,Diode}$	33.5 W	40 W	45.5 W	44.5 W
Total	**67.5 W**	**71.6 W**	**73.7 W**	**70.5 W**

From these results, it is obvious that the performance of a SiC diode has no advantage compared to a Si FRED DSEP12-12A. As SiC SBD's forward voltage drop exhibits positive temperature coefficient, the performance at higher temperatures will change significantly.

Therefore, the calculated losses of the same combinations at T_{vj} = 150°C are listed in **Table 4**.

Table 4. Calculated Semiconductor Losses of tested MOSFET IXFH46N65X3 and Different Diodes in 3-Level T-Type Neutral Boost PFC at T_{vj} = 150°C

@T_J = 150°C	DSEP12-12A	DSEP30-12B	DSEP15-12CR	LSIC2SD120A10
$P_{SW,MOS}$	18.3 W	15.2 W	11.0 W	6.6 W
$P_{cond,MOS}$	54.4 W	54.4 W	54.4 W	54.4 W
$P_{cond,Diode}$	28 W	31 W	36 W	54.4 W
Total	**100.7 W**	**100.6 W**	**101.4 W**	**113 W**

The switching losses of the MOSFET increase by about 25% due to the larger reverse recovery charge of the Si FREDs at higher junction temperatures. For the SiC SBD, the switching losses remain at the same level. However, regarding the overall losses, the situation for SiC SBD gets worse.

Consequently, from these results, the combination consisting of IXFH46N65X3 MOSFET and DSEP12-12A FRED seems practically most promising. The total converter losses at the operating conditions given in **Table 1** can now be calculated according to **equations 6** and **7**:

$$P_{total} = 6 \cdot 67.5\ \text{W} = 405\ \text{W} @\ T_{vj} = 25°\text{C} \quad \textbf{6}$$

$$P_{total} = 6 \cdot 100.7\ \text{W} = 604\ \text{W} @\ T_{vj} = 150°\text{C} \quad \textbf{7}$$

Hence, the expected semiconductor efficiencies are η = 98.17% @ T_{vj} = 25°C and η = 97.26% @ T_{vj} = 150°C.

It can be concluded that the very low switching losses of the Si HiPerDynFRED and SiC SBD do not have significant influence regarding the application performance if the conduction losses dominate. At higher switching frequencies, this behavior will change.

6.1. Estimation of Thermal Performance

Before building prototypes with the selected chips of IXFH46N65X3 and DSEP12-12A, the thermal performance needs to be evaluated first. This is mandatory to verify that the SMPD package can achieve the targeted operating conditions listed in **Table 1**.

Therefore, with the known chip sizes and a thermal path through the well-known Al_2O_3 DCB ceramic of the SMPD package, the resulting thermal resistances including thermal interface material can be estimated as:

$$R_{\text{thJ-HS,MOS}} \approx 0.65\ \text{K/W} \quad (8)$$

$$R_{\text{thJ-HS,Diode}} \approx 2.25\ \text{K/W} \quad (9)$$

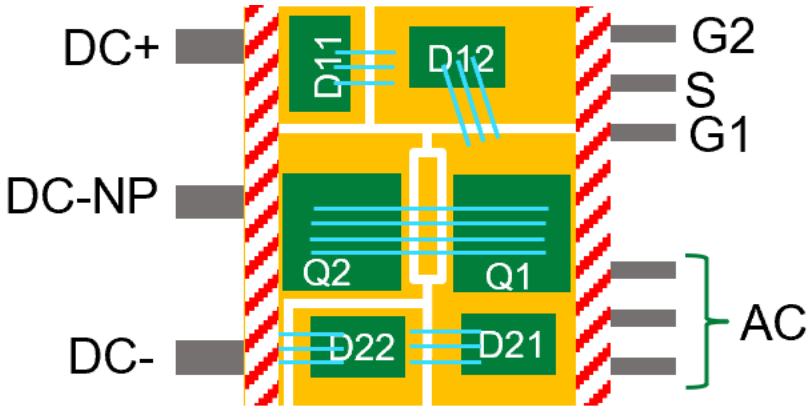
To keep junction temperatures below T_{vj} = 150°C, maximum power losses of $P_{d,MOS}$ = 130.8 W and $P_{d,Diode}$ = 37.8 W can be tolerated. Comparing with the results in **Table 3** and **Table 4**, the maximum junction temperature will not be reached. Consequently, this design can be transferred to the prototyping stage.

6.2. Concept of the DCB Layout

Based on the measurement and calculation results above and besides thermal aspects, a first estimation regarding the mounting area is done via simplified drawing. Rectangular shapes, drawn to scale, enable a first estimation as to whether the dies can be placed onto the available space without obvious violation of design rules.

Figure 10 illustrates the first concept of the DCB without any gate wire bonding.

The layout concept includes further combinations of MOSFETs and series connected diodes such as the HiPerDynFRED. This helps to address different application-specific operating conditions such as higher switching frequencies.



Shaded areas indicate the placing of the lead frame

Figure 10. First DCB Layout Concept and estimation if available DCB Area is sufficient for the Maximum Die Sizes

7. Summary

In this white paper, the design process to integrate a 3-Level T-type Neutral Boost PFC phase-leg into the SMPD package is demonstrated. This white paper presents dynamic characterization results of the silicon Ultrajunction MOSFET IXFH46N65X3 in combination with different silicon FRED technologies to apply those results to the application-related loss estimation and system design. This full silicon solution combines the low cost of silicon with high efficiency without the ultimate need for wide band-gap devices. It can still be argued that SiC or GaN devices will reach lower losses. However, for design engineers, system designers, and supply chain stability reasons, a full silicon solution is still a very good choice, especially in trending topics as, for example, the EV-charging infrastructure.

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