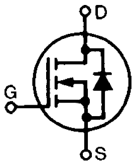
IXYS

TrenchT2™ HiPerFET™ Power MOSFET

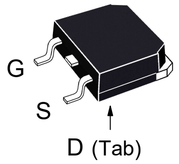
IXFH340N075T2
IXFT340N075T2

V_{DSS} = 75V
I_{D25} = 340A
$R_{DS(on)} \leq$ 3.2mΩ

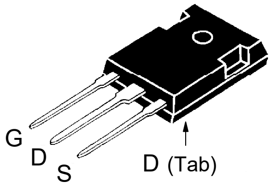
N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



TO-268
(IXFT)



TO-247
(IXFH)



G = Gate
S = Source
D = Drain
Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 175°C	75	V
V_{DGR}	T_J = 25°C to 175°C, R_{GS} = 1MΩ	75	V
V_{GSM}	Transient	± 20	V
I_{D25}	T_C = 25°C (Chip Capability)	340	A
I_{LRMS}	Lead Current Limit, RMS	160	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	850	A
I_A	T_C = 25°C	170	A
E_{AS}	T_C = 25°C	960	mJ
P_D	T_C = 25°C	935	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +175	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	Plastic Body for 10 seconds	260	°C
M_d	Mounting Torque (TO-247)	1.13/10	Nm/lb.in.
Weight	TO-247	6	g
	TO-268	4	g

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	 Typ.	 Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 1mA	75			V
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 3mA	2.0		4.0	V
I_{GSS}	V_{GS} = ± 20V, V_{DS} = 0V			±200	nA
I_{DSS}	V_{DS} = V_{DSS}, V_{GS} = 0V			25	μA
	T_J = 150°C			1.5	mA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 100A, Note 1			3.2	mΩ

Features

- International Standard Packages
- 175°C Operating Temperature
- High Current Handling Capability
- Avalanche Rated
- Fast Intrinsic Diode
- Low $R_{DS(on)}$

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- DC/DC Converters and Off-line UPS
- Primary- Side Switch
- High Current Switching Applications

Symbol	Test Conditions	Characteristic Values			
	(T_J = 25°C, Unless Otherwise Specified)	Min.	Typ.	Max.	
g_{fs}	V_{DS} = 10V, I_D = 60A, Note 1	65	110		S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		19		nF
C_{oss}			2230		pF
C_{rss}			490		pF
R_{Gi}	Gate Input Resistance		1.7		Ω
$t_{d(on)}$	**Resistive Switching Times** V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 100A R_G = 1Ω (External)		26		ns
t_r			50		ns
$t_{d(off)}$			60		ns
t_f			35		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		300		nC
Q_{gs}			68		nC
Q_{gd}			70		nC
R_{thJC}				0.16	°C/W
R_{thCH}	TO-247		0.21		°C/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values			
	(T_J = 25°C, Unless Otherwise Specified)	Min.	Typ.	Max.	
I_S	V_{GS} = 0V			340	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			1360	A
V_{SD}	I_F = 100A, V_{GS} = 0V, Note 1			1.3	V
t_{rr}	I_F = 170A, V_{GS} = 0V -di/dt = 100A/μs V_R = 37.5V		75		ns
I_{RM}			4.4		A
Q_{RM}			165		nC

Note 1. Pulse test, t ≤ 300μs; duty cycle, d ≤ 2%.

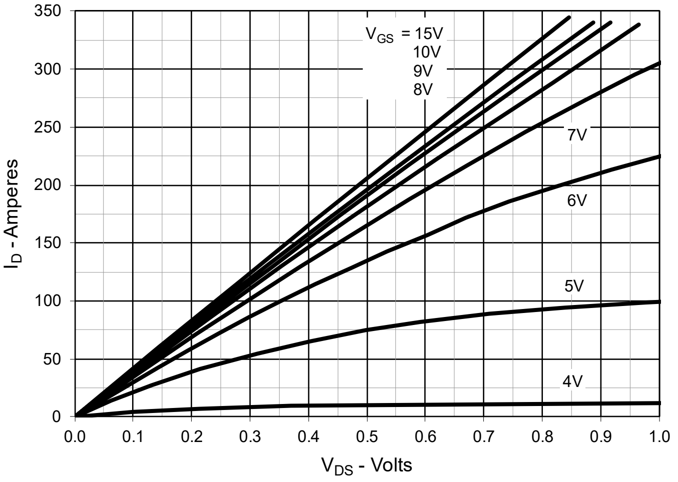


Fig. 1. Output Characteristics @ T_J = 25ºC

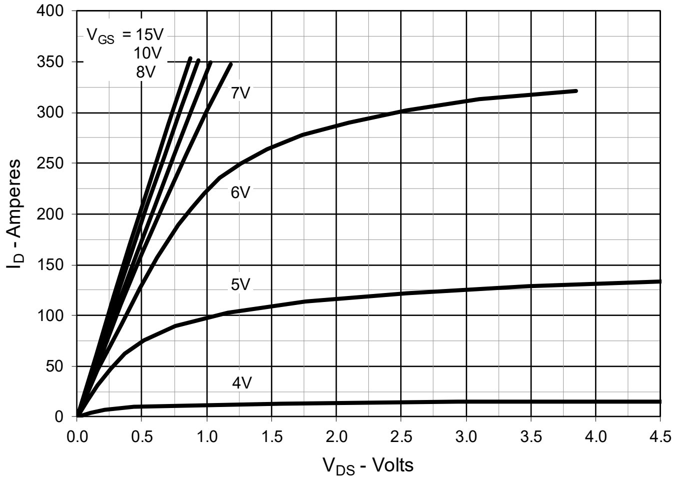


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

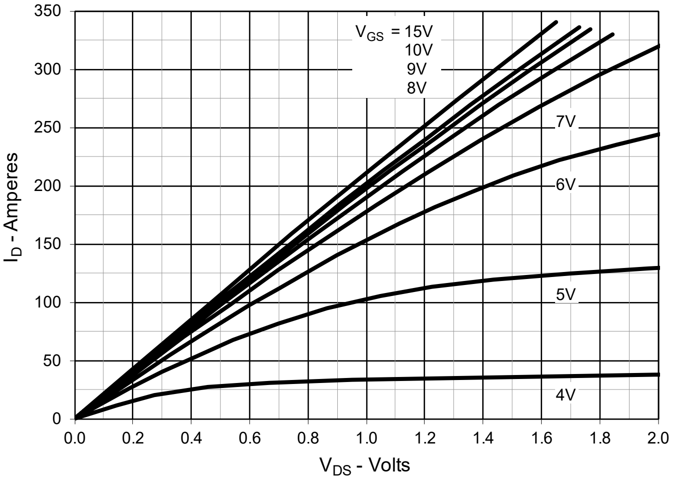


Fig. 3. Output Characteristics @ T_J = 150ºC

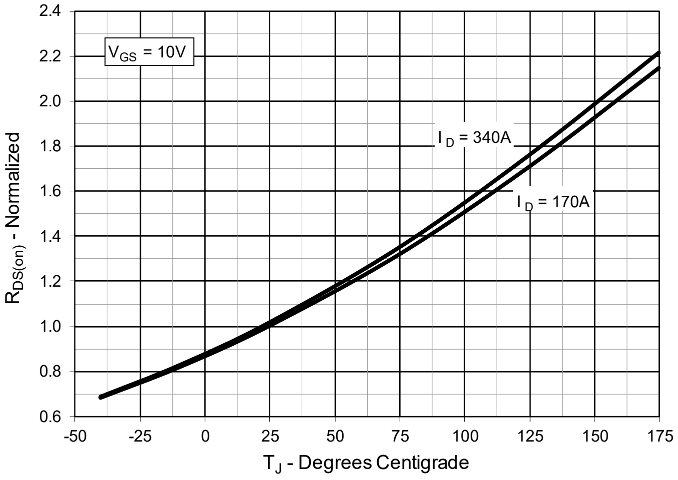


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 170A Value vs. Junction Temperature

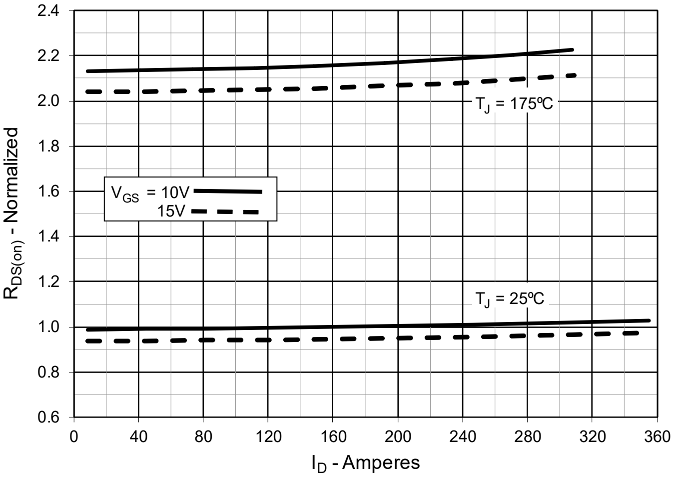


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 170A Value vs. Drain Current

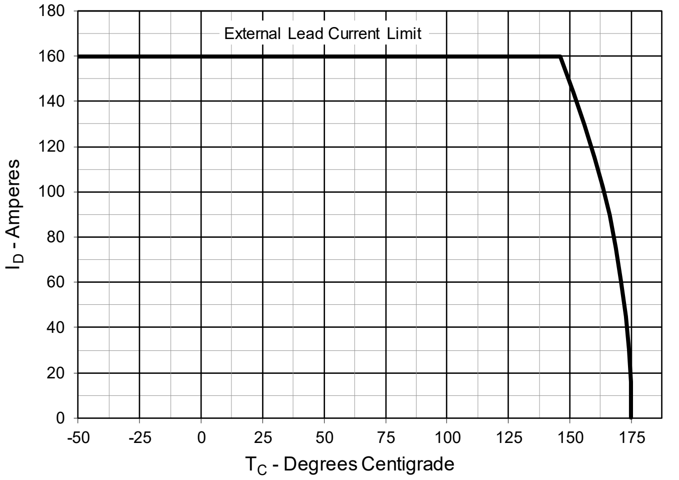


Fig. 6. Drain Current vs. Case Temperature

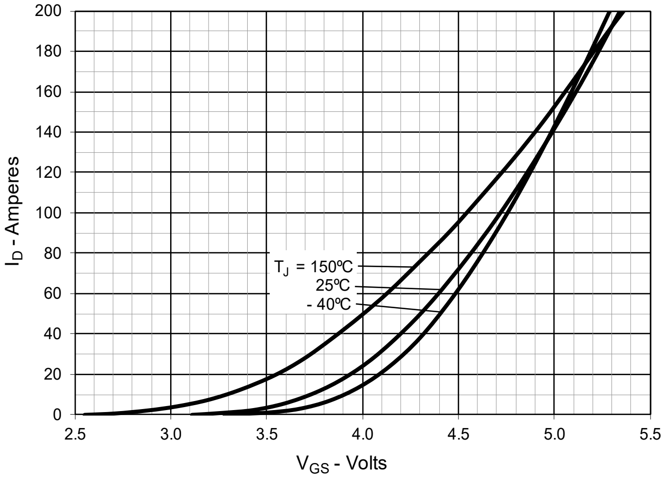


Fig. 7. Input Admittance

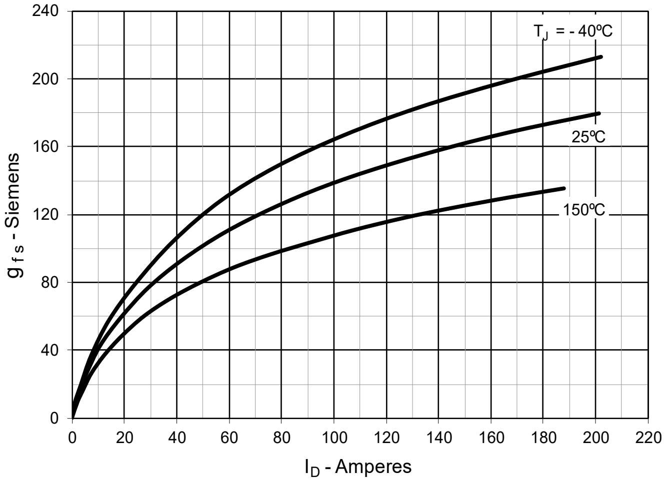


Fig. 8. Transconductance

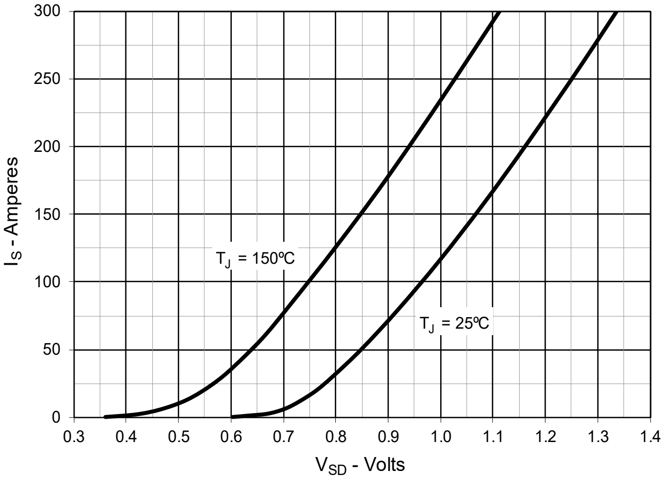


Fig. 9. Forward Voltage Drop of Intrinsic Diode

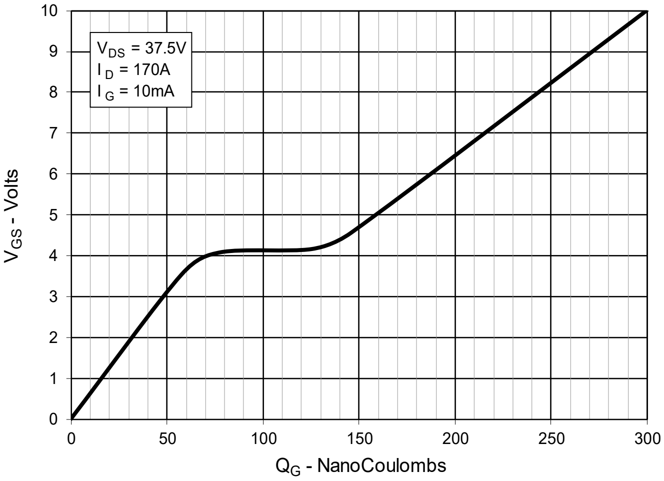


Fig. 10. Gate Charge

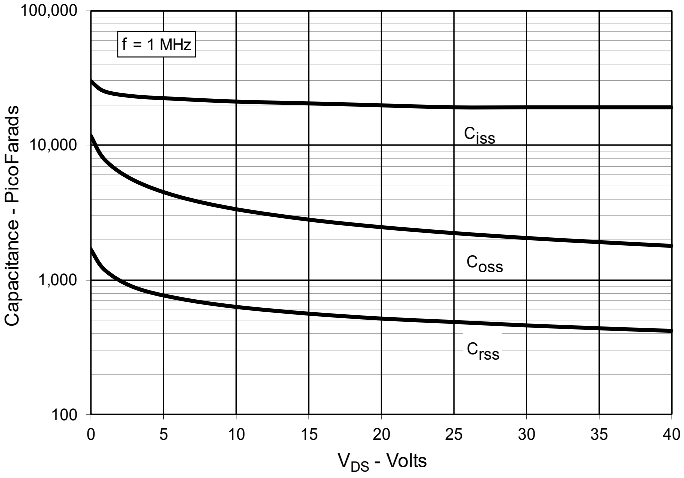


Fig. 11. Capacitance

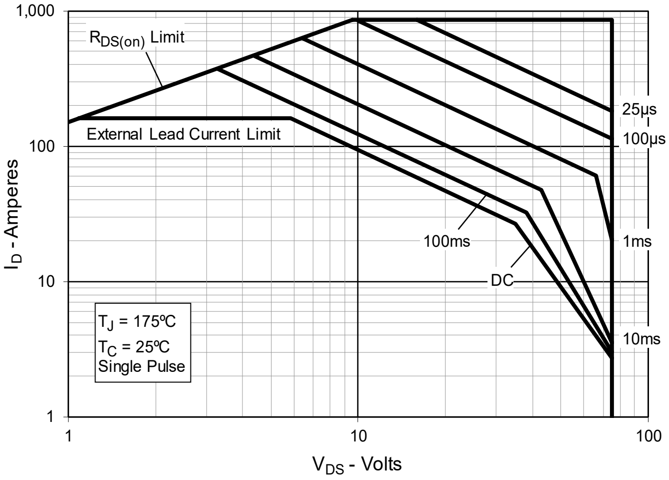


Fig. 12. Forward-Bias Safe Operating Area

Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

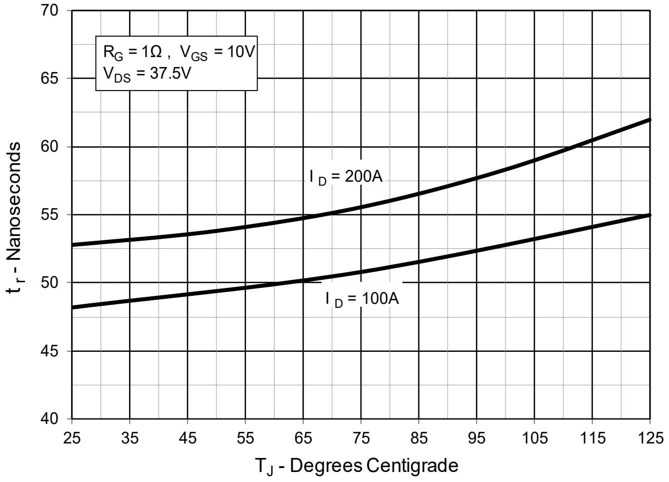


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

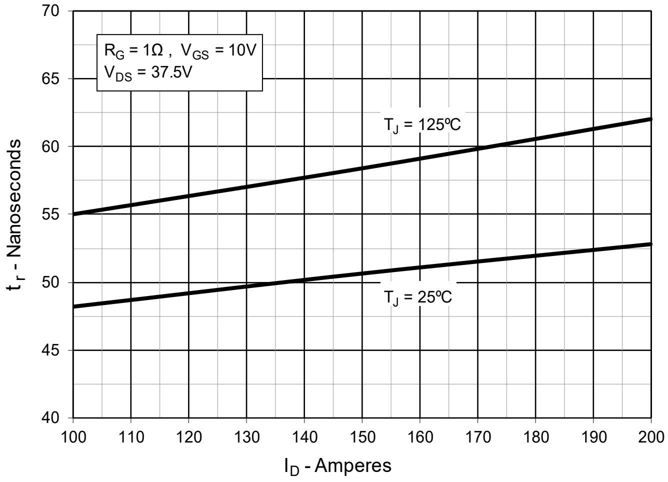


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

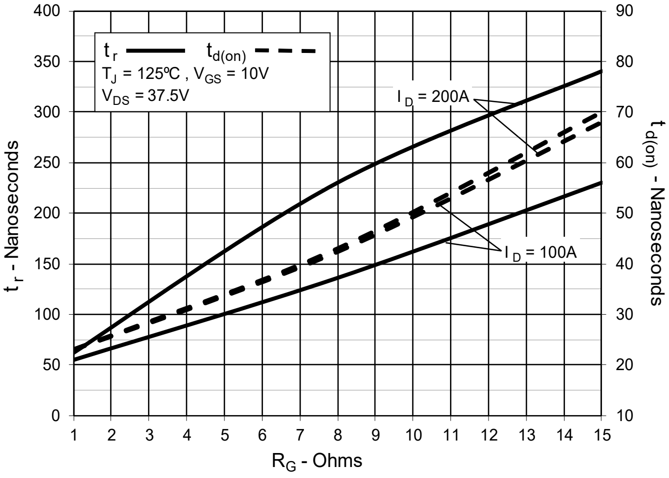


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

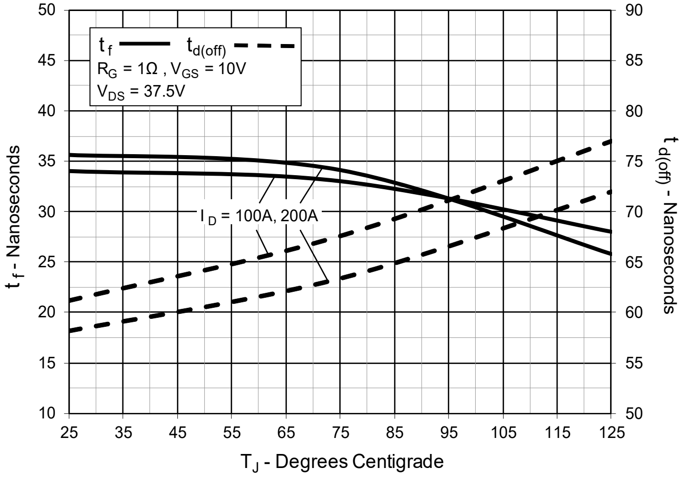


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

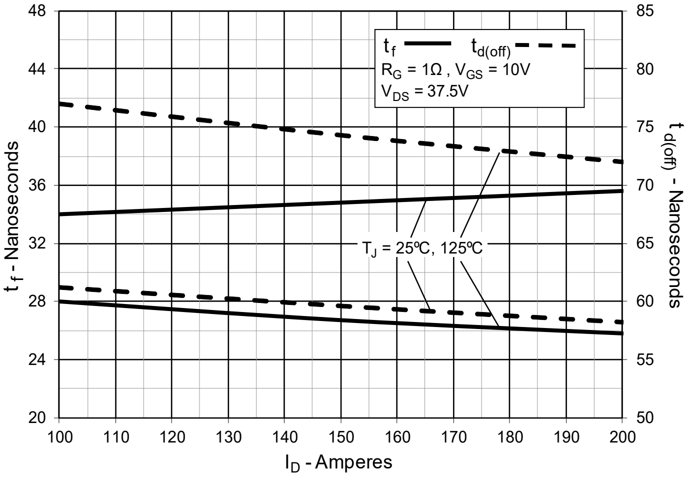


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

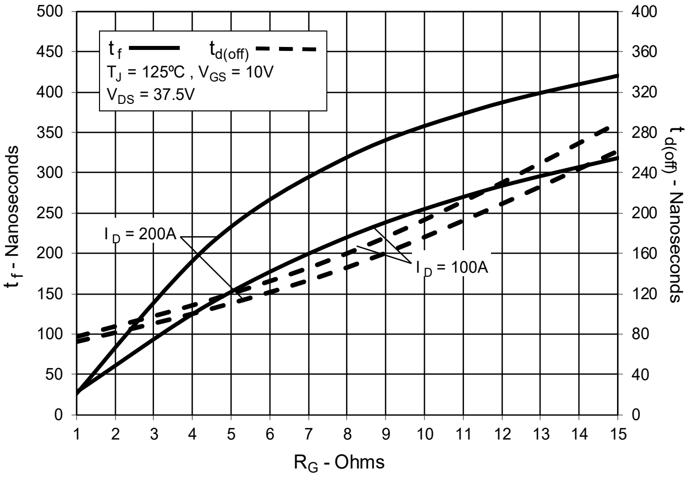
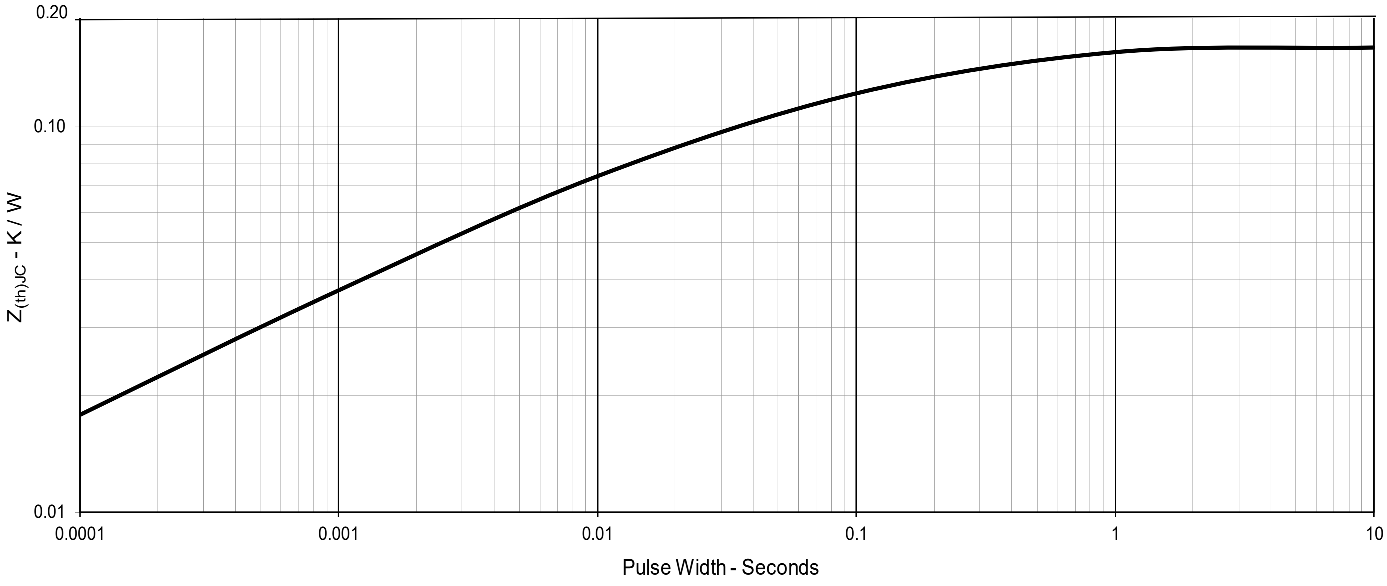
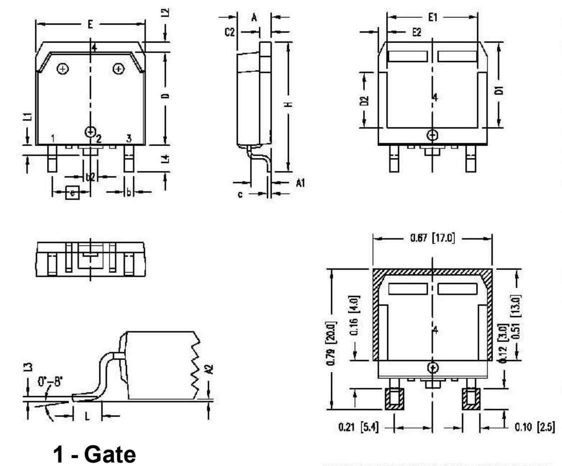


Fig. 19. Maximum Transient Thermal Impedance



IXYS REF: F_340N075T2 (V8) 5-18-21

TO-268 Outline

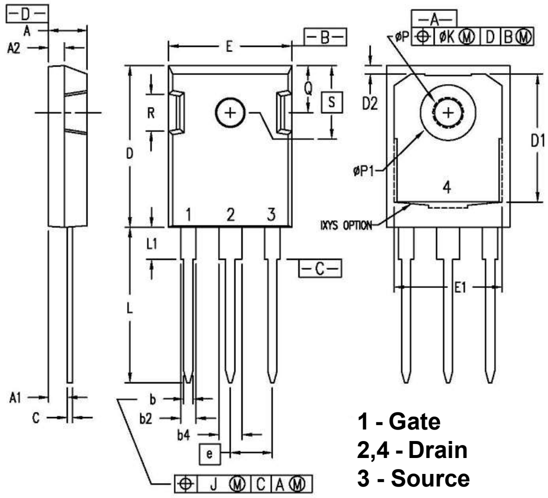


1 - Gate
2,4 - Drain
3 - Source

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
D2	.320	.335	8.13	8.50
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
E2	.045	.055	1.14	1.39
e	.215 BSC		5.45 BSC	
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010 BSC		0.25 BSC	
L4	.150	.161	3.80	4.10

NOTE: ALL METAL SURFACE ARE MATTE PURE TIN PLATED EXCEPT TRIM AREA.
Pb PLATING THICKNESS (4 – 20 um)

TO-247 Outline



1 - Gate
2,4 - Drain
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.087	1.91	2.20
b4	.115	.126	2.92	3.20
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
D1	.650	.690	16.51	17.53
D2	.035	.050	0.89	1.27
E	.620	.635	15.75	16.13
E1	.545	.565	13.84	14.35
e	.215 BSC		5.45 BSC	
J	--	.010	--	0.25
K	--	.025	--	0.64
L	.780	.810	19.81	20.57
L1	.150	.170	3.81	4.32
øP	.140	.144	3.55	3.65
øP1	.275	.290	6.99	7.37
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.242 BSC		6.15 BSC	

NOTE: This drawing will meet all dimensions requirement of JEDEC outlines TO-247 AD (R-PSIP-F3)

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