IXYS

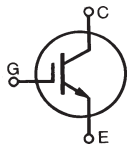
Advance Technical Information

GenX3™ 1000V IGBTs

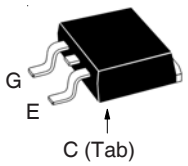
IXGA20N100A3
IXGP20N100A3
IXGH20N100A3

V_{CES} = 1000V
I_{C90} = 20A
$V_{CE(sat)} \leq$ 2.3V

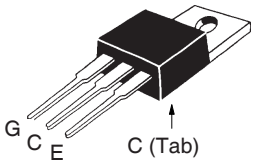
Ultra-Low Vsat PT IGBTs for up to 3kHz Switching



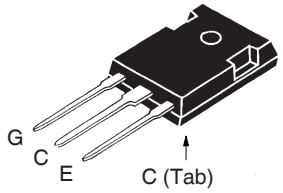
TO-263 (IXGA)



TO-220 (IXGP)



TO-247 (IXGH)



G = Gate C = Collector
E = Emitter Tab = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	1000	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	1000	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	40	A
I_{C90}	T_C = 90°C	20	A
I_{CM}	T_C = 25°C, 1ms	100	A
SSOA (RBSOA)	V_{GE} = 15V, T_J = 125°C, R_G = 50Ω Clamped Inductive Load	I_{CM} = 40 @ $V_{CE} \leq$ 800	A V
P_C	T_C = 25°C	150	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
M_d	Mounting Torque (TO-247 & TO-220)	1.13/10	Nm/lb.in.
F_C	Mounting Force (TO-263)	10..65 / 2.2..14.6	N/lb.
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6mm (0.062 in.) from Case for 10s	260	°C
Weight	TO-263	2.5	g
	TO-220	3.0	g
	TO-247	6.0	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	1000			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}	2.5		5.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			25	μA
	T_J = 125°C			500	μA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±100	nA
$V_{CE(sat)}$	I_C = 20A, V_{GE} = 15V, Note 1		2.1	2.3	V
	T_J = 125°C		2.3		V

Features

- Optimized for Low Conduction Losses
- International Standard Packages

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

- Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts
- Inrush Current Protection Circuits

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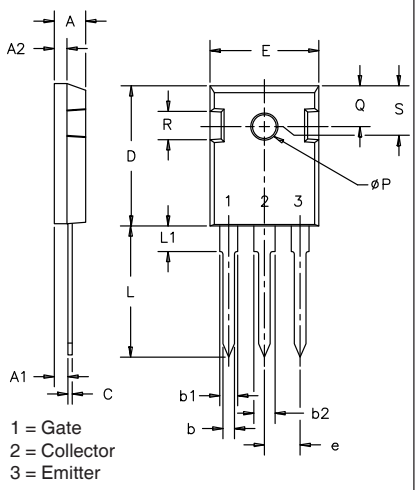
Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	I_C = 20A, V_{CE} = 10V, Note 1	9	16	S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		1110	pF
C_{oes}			56	pF
C_{res}			15	pF
$Q_{g(on)}$	I_C = 20A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		40.0	nC
Q_{ge}			6.7	nC
Q_{gc}			15.5	nC
$t_{d(on)}$	**Resistive Switching Times, T_J = 25°C**		34	ns
t_r	I_C = 20A, V_{GE} = 15V		110	ns
$t_{d(off)}$	V_{CE} = 800V, R_G = 10Ω		75	ns
t_f			1090	ns
$t_{d(on)}$	**Resistive Switching Times, T_J = 125°C**		37	ns
t_r	I_C = 20A, V_{GE} = 15V		125	ns
$t_{d(off)}$	V_{CE} = 800V, R_G = 10Ω		80	ns
t_f			1550	ns
R_{thJC}				0.83 °C/W
R_{thCK}	TO-220		0.50	°C/W
	TO-247		0.21	°C/W

Note:

1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

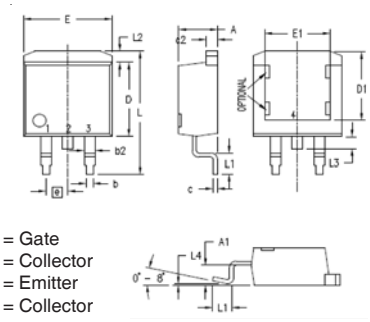
TO-247 Outline



1 = Gate
2 = Collector
3 = Emitter

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.209	4.7	5.3
A_1	.087	.102	2.2	2.54
A_2	.059	.098	2.2	2.6
b	.040	.055	1.0	1.4
b_1	.065	.084	1.65	2.13
b_2	.113	.123	2.87	3.12
C	.016	.031	.4	.8
D	.819	.845	20.80	21.46
E	.610	.640	15.75	16.26
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1		.177		4.50
øP	.140	.144	3.55	3.65
Q	.212	.244	5.4	6.2
R	.170	.216	4.32	5.49
S	.242 BSC		6.15 BSC	

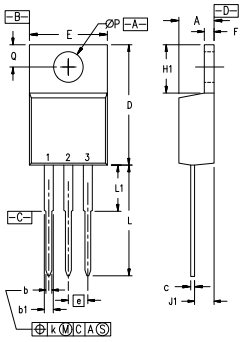
TO-263 Outline



1 = Gate
2 = Collector
3 = Emitter
4 = Collector

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.160	.190	4.06	4.83
A1	.080	.110	2.03	2.79
b	.020	.039	0.51	0.99
b2	.045	.055	1.14	1.40
c	.016	.029	0.40	0.74
c2	.045	.055	1.14	1.40
D	.340	.380	8.64	9.65
D1	.315	.350	8.00	8.89
E	.380	.410	9.65	10.41
E1	.245	.320	6.22	8.13
e	.100 BSC		2.54 BSC	
L	.575	.625	14.61	15.88
L1	.090	.110	2.29	2.79
L2	.040	.055	1.02	1.40
L3	.050	.070	1.27	1.78
L4	0	.005	0	0.13

TO-220 Outline



Pins: 1 - Gate 2 - Collector
3 - Emitter

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
øP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ T_J = 25ºC

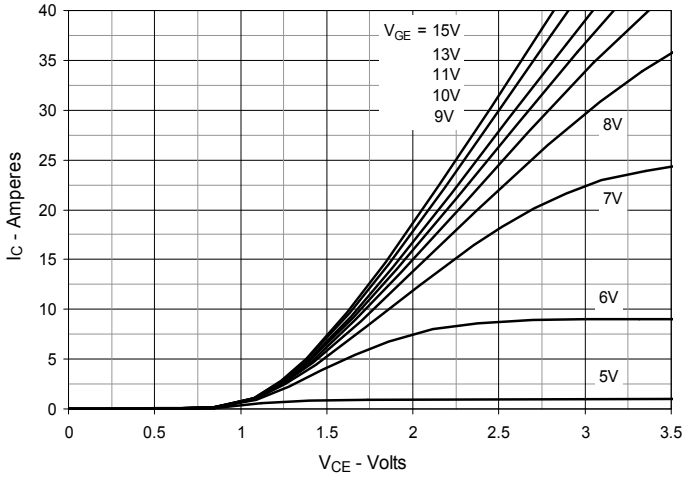


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

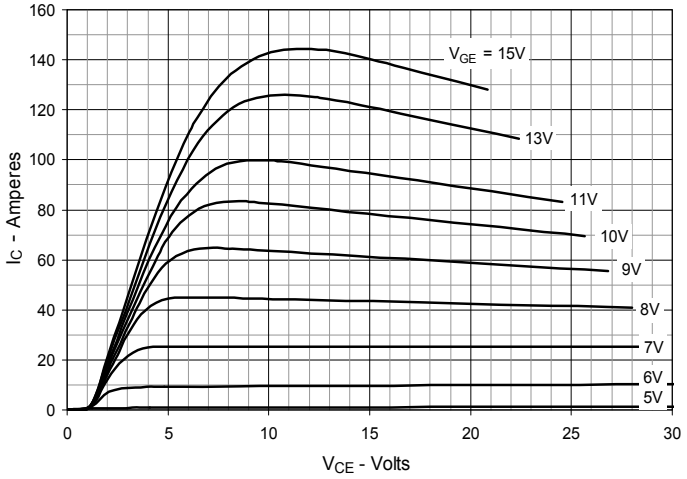


Fig. 3. Output Characteristics @ T_J = 125ºC

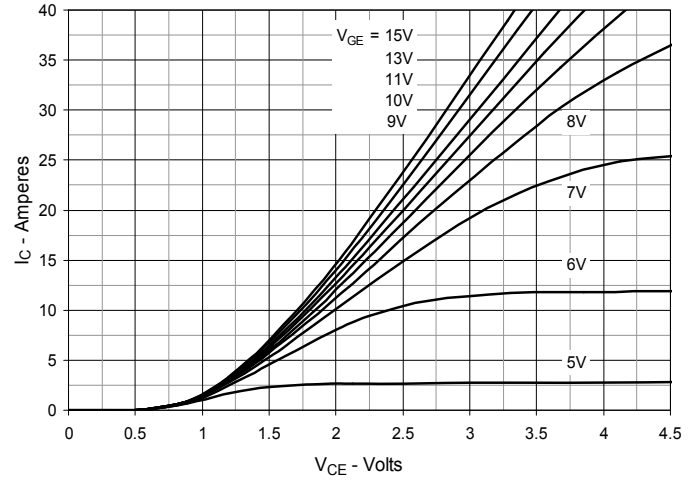


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

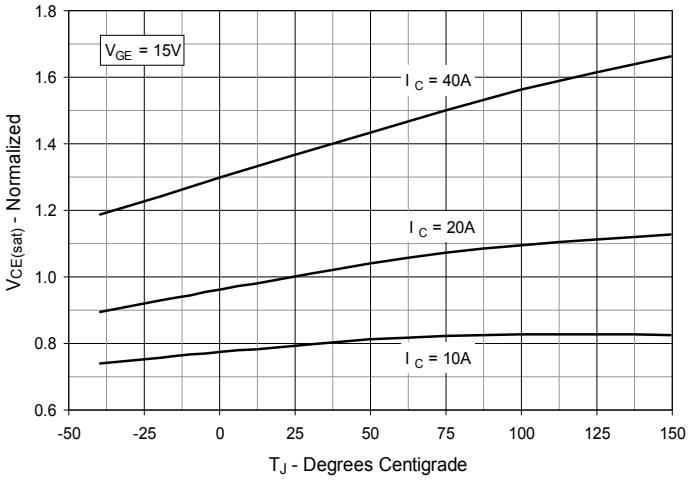


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

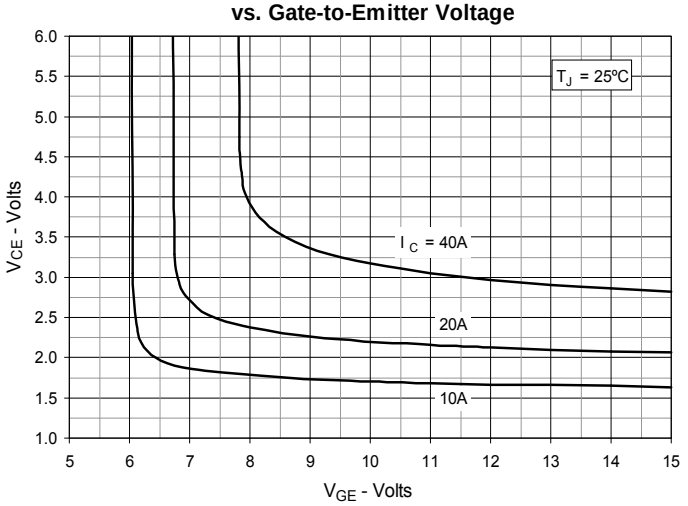


Fig. 6. Input Admittance

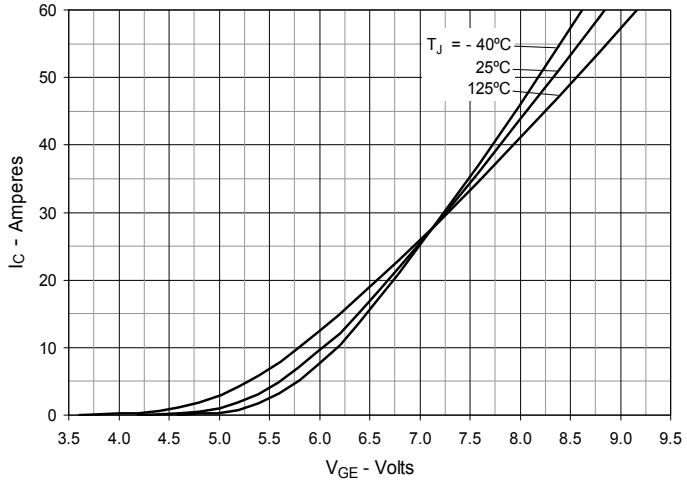


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Fig. 7. Transconductance

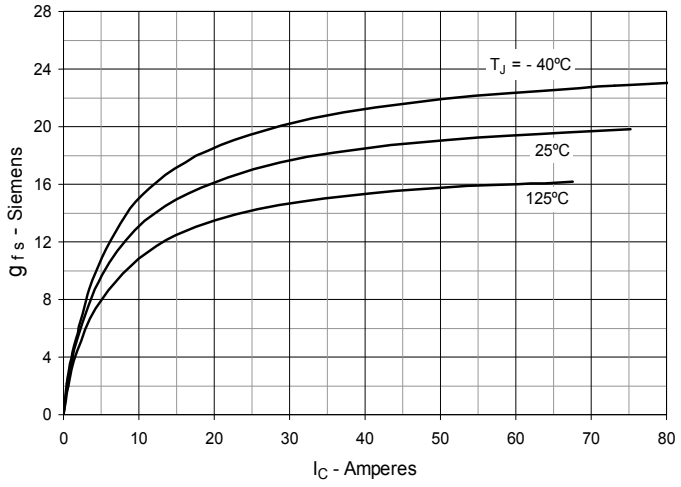


Fig. 8. Gate Charge

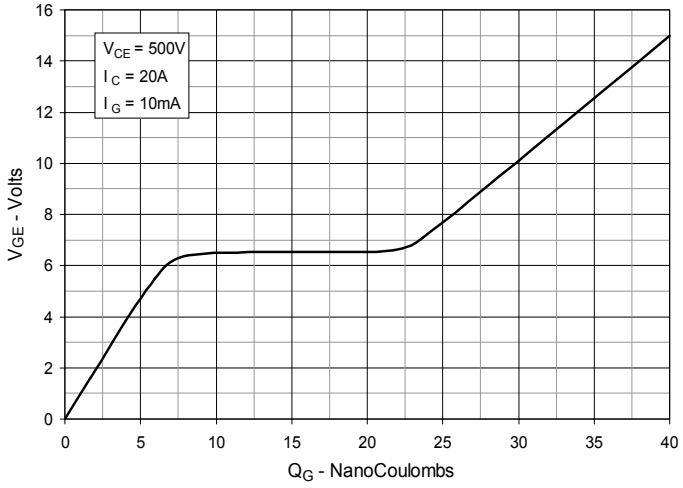


Fig. 9. Reverse-Bias Safe Operating Area

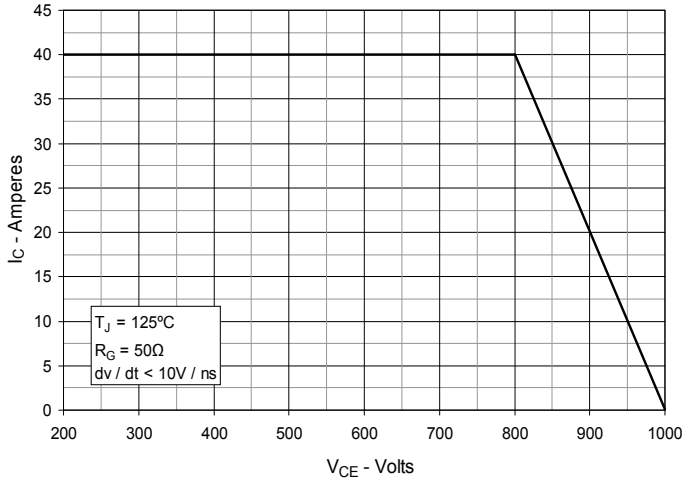


Fig. 10. Capacitance

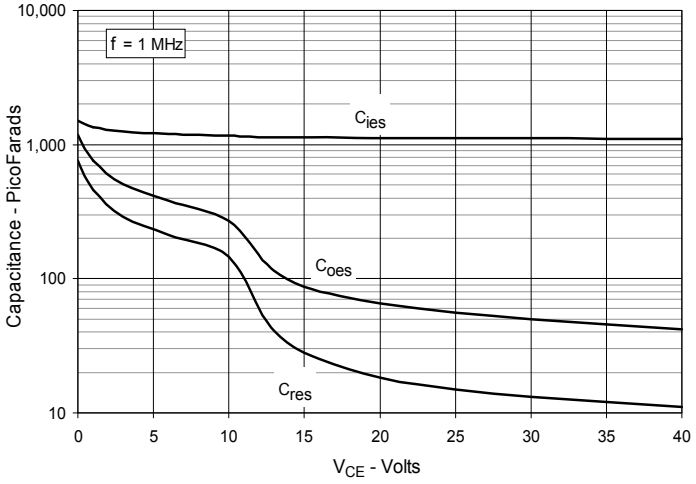
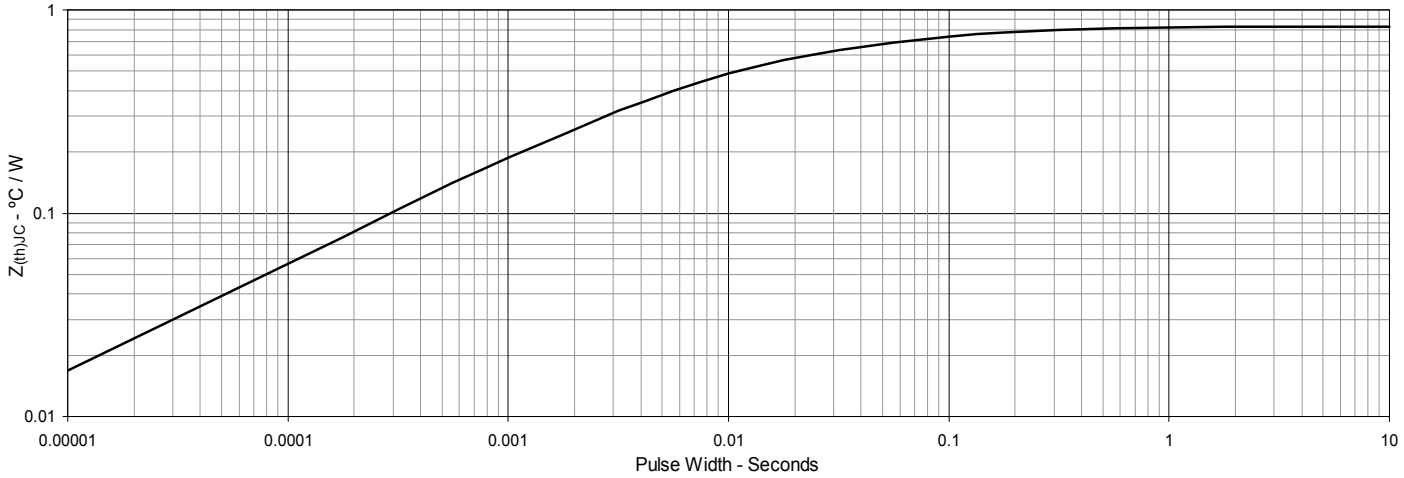


Fig. 11. Maximum Transient Thermal Impedance



IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

Fig. 12. Resistive Turn-on Rise Time vs. Junction Temperature

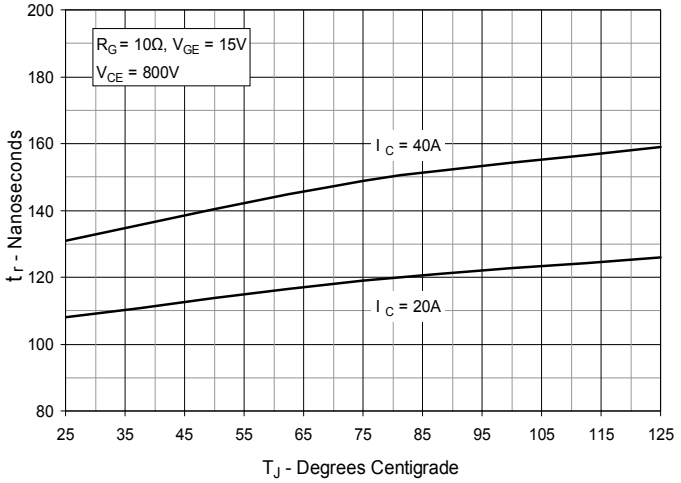


Fig. 13. Resistive Turn-on Rise Time vs. Collector Current

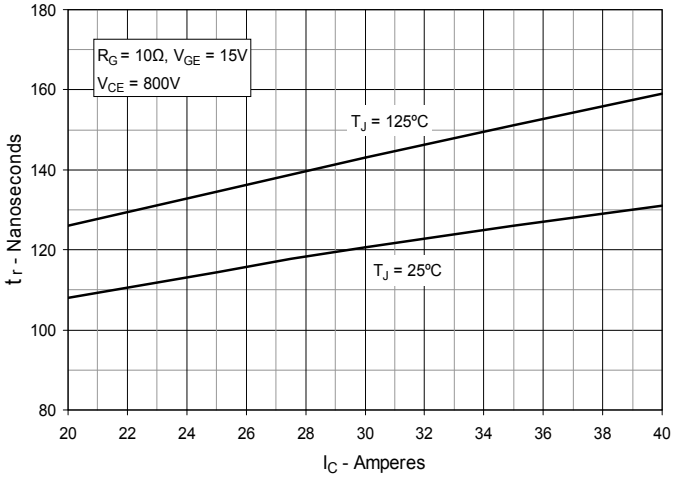


Fig. 14. Resistive Turn-on Switching Times vs. Gate Resistance

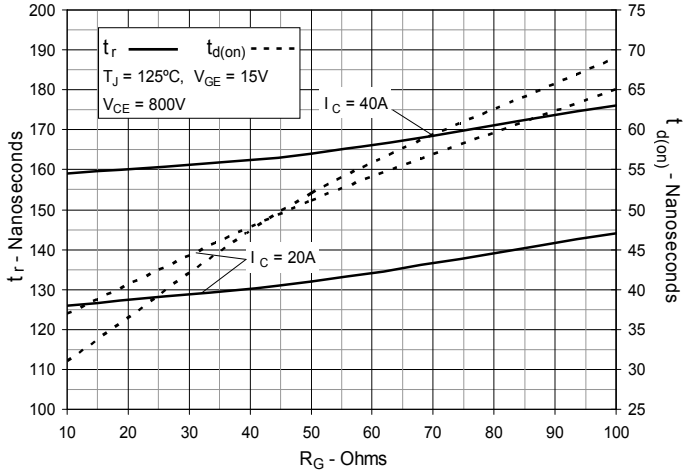


Fig. 15. Resistive Turn-off Switching Times vs. Junction Temperature

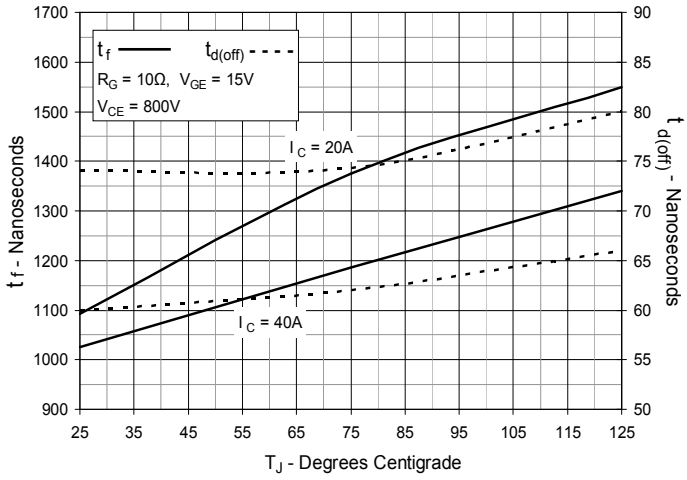


Fig. 16. Resistive Turn-off Switching Times vs. Collector Current

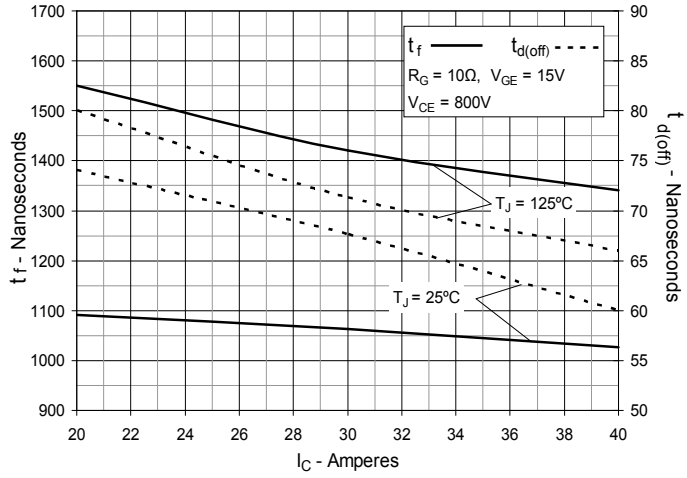
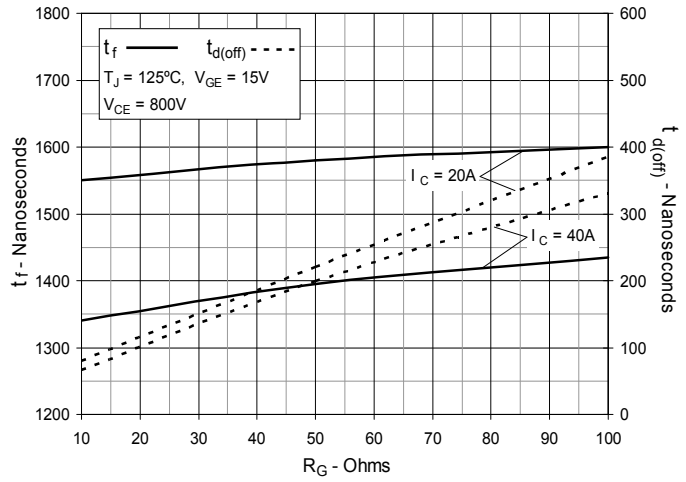


Fig. 17. Resistive Turn-off Switching Times vs. Gate Resistance



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