TECH
BRIEF

ESD Protection
Digital Visual Interface Data Lines

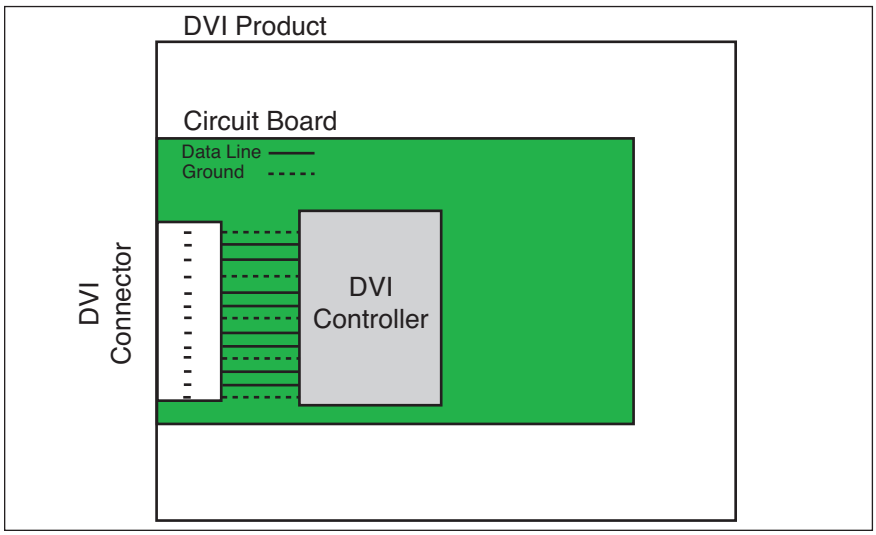

Figure 1. Simple DVI circuit diagram (ESD suppressors protect the data lines which have exposure to the outside world. The DVI protocol uses 8 high-speed data/clock lines).

Background

Digital Visual Interface (DVI) products (source and display units) can be susceptible to ESD events when the cable is disconnected from the data port. The ESD pulse can be introduced directly into the open port, or into the disconnected end of the cable. Either way, the integrated circuitry that controls the DVI system functionality can be compromised.

The Problem

After the ESD pulse is introduced into the data/clock port, it will travel through the connector to the PC board. Once on the PC board, it will propagate down these lines toward the integrated circuitry. Specifically, the IC of concern is the **DVI Controller**. Without sufficient protection, the Controller chip can be rendered inoperable.

The Solution

In order to provide the IC with protection against ESD transients, the use of suppression products is recommended. The suppressors are installed between the data/clock line and the chassis ground (parallel connection) and shunt the ESD transient from line to ground.

For high-speed protocols like that of DVI (1.12 Gbps), suppressors with extremely low capacitance levels should be used. Suppressors with high capacitance can affect the data stream by distorting the data waveforms

Littelfuse offers PulseGuard® ESD suppressors as a solution for DVI data/clock line ESD protection. These products are surface mount devices with 0.050 pF of capacitance. So they will provide ESD protection and maintain the integrity of the data signals.

Examples of DVI products which can benefit from ESD protection include:

Visual Sources
- Desktop and laptop computers
- DVD's and PVR's
- Set top boxes

Visual Displays
- LCD and CRT units
- LCD overhead projector
- HDTV monitors





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Capacitance and Signal Integrity

In previous generations of I/O protocols (RS232, USB 1.1, 10BaseT, etc.), the signal speed (rise/fall time of logic states) was sufficiently slow that the parasitic components of circuit protection devices was of minimal concern.

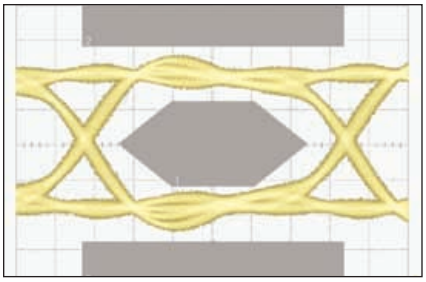

Figure 2. Control Signal (No devices added)

However, as data rates have increased, the capacitive loading that is presented to the data circuitry by the protection device becomes more of a concern. For example, the diagrams below show the effect capacitive loading has on a high-speed (2.5 Gbps) waveform.

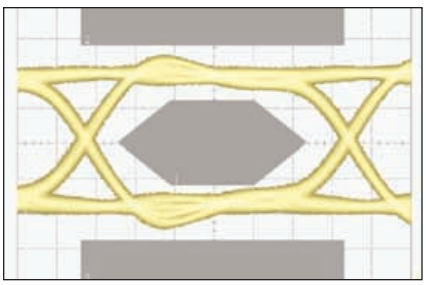

Figure 3. PulseGuard® suppressor (0.05pF) added to data line

The first diagram shows the eye diagram for a control board which only contains a the data lines. The second diagram shows the response of the data line which has a PulseGuard® ESD suppressor installed. The third diagram is included for reference, and shows the response when a 3 pF capacitor is installed on the data line. The PulseGuard device and capacitor were reference to ground.

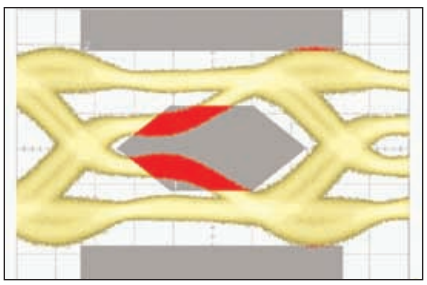

Figure 4. Surface mount capacitor (3pF) added to data line

The signals replicate the InfiniBand℠ protocol (1.0 - 1.6V, 2.5 Gbps); created on Agilent BERT equipment and measured with an Agilent Infinium DCA. The InfiniBand protocol is similar to the DVI protocol in that multiple, low voltage, differential pairs are used to transmit the overall data stream. Since the PulseGuard low capacitance product does not interfere with the faster 2.5 Gbps data rate, it will also not interfere with the integrity of the DVI (1.12 Gbps) data stream.

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