SP720, SP721 and SP723 Turn-On and Turn-Off Characteristics

Application Note | March 1997 | AN9708

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Introduction

The purpose of this Application Note is to focus on customer concerns related to the fast switching characteristics of the SP720, SP721 and SP723 family of protection ICs during an ESD discharge. The SCR cell structures of this family were first introduced for ESD protection of sensitive ICs that were subject to substantially more severe conditions than normal Human Body Model stress. The primary ESD protection requirement of the SCR structure is to absorb and divert energy away from the signal interface of sensitive circuits. Shown in Figure 1, each active input has a pair of SCRs to provide dual polarity protection directly in the signal interface.

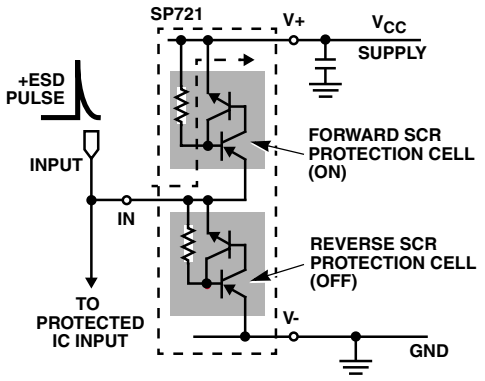


FIGURE 1. AN ILLUSTRATION OF SP721 ESD PROTECTION FOR A POSITIVE ESD PULSE, THE FORWARD SCR CELL CONDUCTS CURRENT TO THE V_{CC} SUPPLY

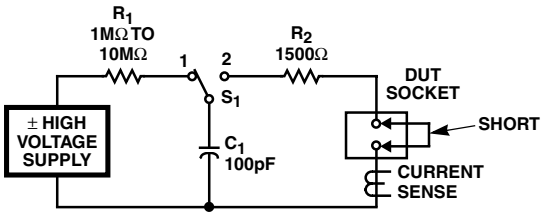
To meet the needs of a high performance application, a protection device must have a wide dynamic operating range with minimal loading. The SP720, SP721 and SP723 have a wide dynamic operating range of 35V with low input capacitance and low leakage while still providing the rugged level of protection necessary for most signal interface requirements. Low capacitance loading is essential for a fast ESD protection response time. The input capacitance of the SP720 and SP721 is typically 3pF and for the SP723 is 5pF. Each IN input has typically 5nA of leakage and the quiescent power supply current has 50nA of current.

The SCR cell structure was chosen for both a fast turn-on response and a low series resistance path to the high current of an ESD discharge. The SCR has a characteristic of decreasing resistance with increasing current, typically decreasing to 1Ω at 2A peak current. Positive and negative SCR cells are paired to work as active switches. The energy of an ESD discharge is both absorbed and shunted by the SCR to the supply line (positive pulse) or ground (negative pulse). When the energy is dissipated, the SCR quickly returns to its off state because there is no current to sustain the latched holding condition of the SCR.

Turn-On Time of the SP721AP

Figure 1 shows the paired SCR cell configuration of the SP721 with an illustration of how it responds to a positive ESD pulse applied to the input. The top or forward SCR cell responds to a positive ESD pulse and turns on when the voltage at the IN input is one V_{BE} greater than the voltage of the V+ terminal. ESD pulse current is conducted from the IN input to V+. The V+ of the SP721 is common to the V_{CC} power supply line of the IC being protected. The SCR begins to conduct in ~0.7ns and has a typical turn-on delay time of 2ns.

To illustrate the turn-on characteristic and speed of the SCR, Figure 2 shows the Human Body Model ESD pulse simulator per MIL-STD-883D, Method 3015.7. This circuit discharges a 100pF capacitor through 1500Ω to a device under test (DUT). The waveform Turn-ON characteristic for current vs. time of an SP72/1 when activated by a +2kV ESD pulse is shown in Figure 3. The SP720, SP721 and SP723 have the same cell design and turn-on characteristic.



SWITCH S_1 IN POSITION 1 CHARGES CAPACITOR C_1. WHEN S_1 IS SWITCHED TO POSITION 2, CAPACITOR C_1 DISCHARGES INTO R_1 AND THE DEVICE UNDERTEST (DUT). THE DUT SOCKET IS SHORTED PIN-TO-PIN FOR SIMULATOR WAVEFORM VERIFICATION. AN OSCILLOSCOPE CURRENT PROBE IS USED TO SENSE THE DISCHARGE CURRENT WAVEFORM.

FIGURE 2. MIL-STD-883D, METHOD 3015.7 ESD TEST CIRCUIT SHOWING THE CURRENT WAVEFORM VERIFICATION SETUP FOR THE HBM TEST FIXTURE

Figure 3 shows waveforms of switching time vs current for the SP721. The top display is a full scale view of an SP721 ESD discharge waveform vs a reference short circuit (calibration) discharge waveform for the test fixture of Figure 2. The bottom display is an expanded view for both curves with the same zero reference for the SP721 turn-on waveform “B” vs the input reference waveform “A”. (The zero baselines of both waveforms are initially offset 0.35ns by the threshold of the scope trigger level.) The turn-on delay of the SP721 SCR increases to just over 2ns from the reference input waveform “A” and then drops back to less than 2ns.

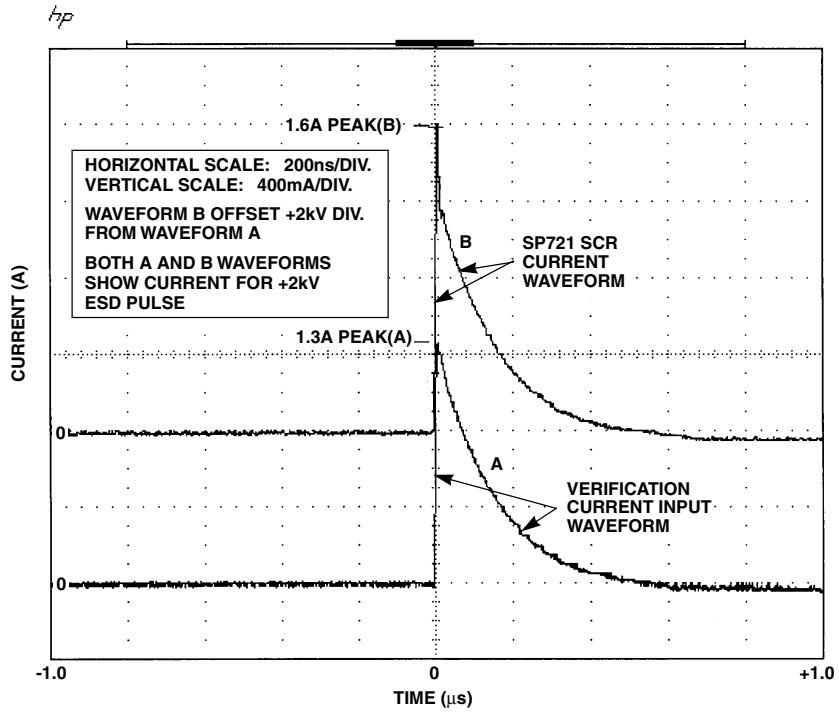


FIGURE 3A.

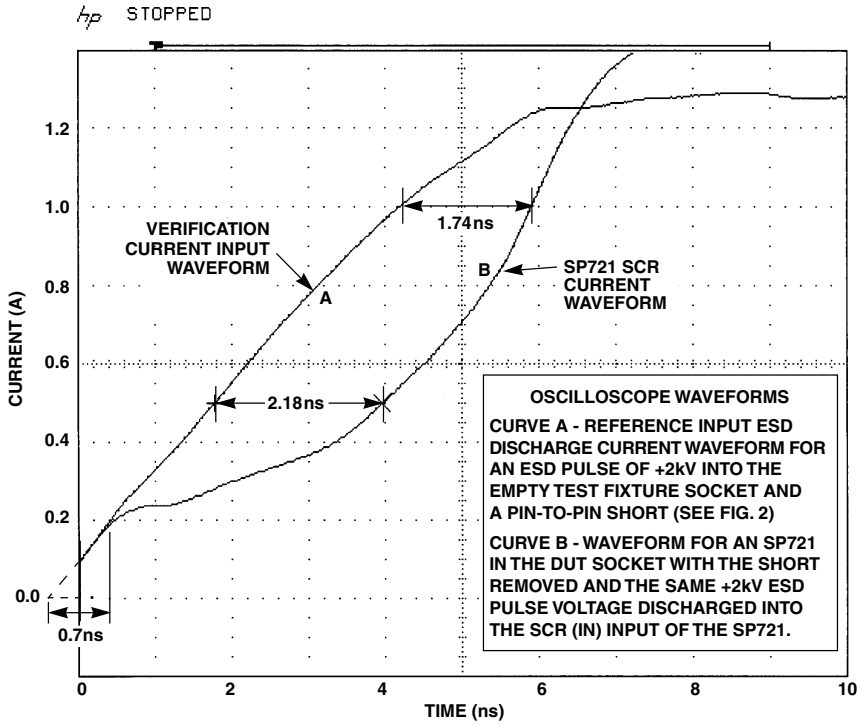


FIGURE 3B.

FIGURE 3. OSCILLOSCOPE WAVEFORMS SHOWING CURRENT vs TIME FOR THE MIL-STD-883D, METHOD 3015.7 TEST CIRCUIT OF FIGURE 2. FIGURE 3A IS A FULL SCALE OF ESD DISCHARGE TIME AS SHOWN ON A HP54540A DIGITAL OSCILLOSCOPE. FIGURE 3B SHOWS AN EXPANDED VIEW WITH AN OVERLAY OF THE REFERENCE OR SHORTED FIXTURE WAVEFORM "A" FOR VERIFICATION (CALIBRATION) AND WAVEFORM "B" AS THE SCR TURN-ON AND DELAY TIME RESPONSE. THE SCR TURN-ON DELAY TIME IS TYPICALLY 2ns.

The 1500Ω of the standard test circuit should allow an initial peak current of 1.33A when the capacitor C_1 charge is 2kV. Current through the SP721 peaks at 1.6A and is then quickly damped. Lead inductance and stray capacitance at the input causes some transient ringing and overshoot. After a few nanoseconds of ringing, the fall time of the SP721 current waveform "B" (shown in the top display) is identical to the reference waveform "A".

Speed vs ESD Rated Capability

For any application, the maximum rated ESD capability is most desirable. However, this is a trade-off with performance related parameters such frequency (Mb or MHz), static or dynamic impedance and stability. The SP720, SP721 and SP723 offer an optimal trade-off, having high HBM ESD voltage capability to both MIL-STD-883 and IEC 1000-4-2 standards with very low capacitance and are designed to work in the signal interface to protect sensitive ICs. Many competitive ESD protection products have high capacitance and can only be used for power supply or power line protection.

SCR Structure vs a Zener Device

What is the advantage of the SCR over a Zener diode? While it is relative simple to suggest that Zener diode may offer more capability, increasing area for improved ESD ratings increases the capacitance of the Zener junction. When a Zener becomes active, dissipation at the junction is the Zener voltage times the current. When the SCR structure becomes active, it latches on with low resistance and low internal dissipation.

SCR Unlatch Speed

The SCR quickly unlatches when the current drops to zero. Figure 3A shows the full waveform for turn-on and turn-off time. The SP721 waveform "B" closely follows the reference input waveform "A". Delay in the SCR turn-off is not significantly longer than the disruptive period of the simulated ESD pulse.

Latch

It should be noted that "latch" as referenced in the turn-on of the SCR has no relation to latching input problems that were common in older CMOS devices and may occasionally occur as an irregularity in other processes. The SCR cells are designed to latch on with a disruptive signal that is greater than the supply voltage (V+) or less than ground (V-). The SCR falls out of latch when input voltage returns to a normal mode of operation.

How Best to Protect a CMOS IC Input

Figure 4 illustrates an SP720, SP721 or SP723 interface with a typical CMOS IC input circuit. This example shows a typical input for high speed CMOS which includes an internal series resistor R_P to stacked protection diodes, followed by a resistor and diode. R_P is typically an integral polysilicon resistor with a resistance of 120Ω and can be subjected to ESD damage for voltage levels higher than 2kV. Use of an SP720, SP721 or SP723 will substantially improve the signal line input against an ESD discharge.

While the conducting SCR will clamp an ESD pulse, the discharge current will cause some ride-up of the voltage on the signal input line. For example, an HBM ESD discharge of +3kV (see Figure 2) will cause approximately 2A of current. With this positive input current, the input voltage will exceed the V_{CC} level and turn-on the forward SCR. The data sheet I-V curve indicates that the forward voltage drop of the SCR for 2A will be typically 3V. As such, it is recommended that a series resistor be used at the CMOS input (shown here as R_1). This will add resistance to limit current into the CMOS IC by forming a current divider with the latched-on SCR. Without R_1, diode D_1 would see a 3V forward turn-on or (3V - 0.7V)/(120) = 19.2mA. A typically HC CMOS should tolerate twice this level. However, an external resistor of 120Ω would further reduce the current by one-half. An IC with a 2kV rated input can be protected to 10kV or higher, depending on the CMOS internal network and resistor, R_1.

It is recommended to use the largest value of R_1 that is permitted, consistent with the trade-off in circuit performance. In layout, it is also recommended to keep the signal line input layout as short as possible to minimize ringing and transients caused by stray inductance and capacitance.

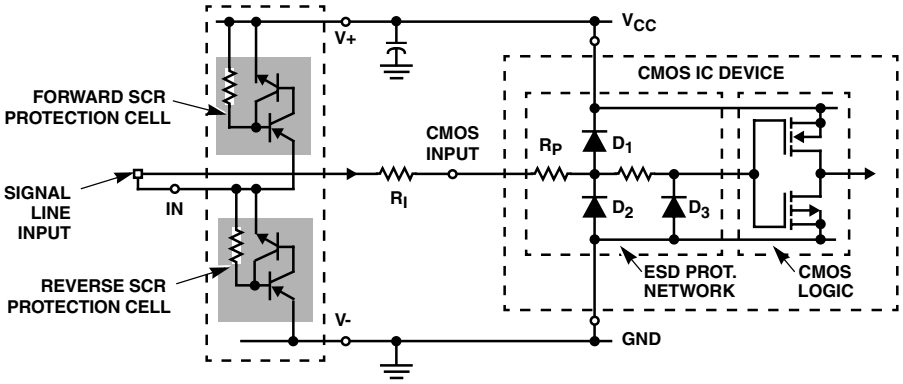


FIGURE 4. SP720, SP721 OR SP723 SCR INTERFACE TO A CMOS INPUT WITH R_I ADDED TO ILLUSTRATE MORE EFFECTIVE ESD PROTECTION FOR CMOS DEVICES