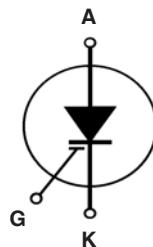
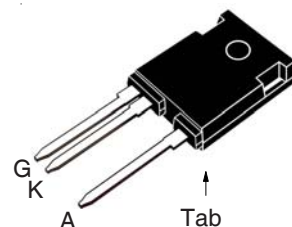


1500V MOS Gated Thyristor

IXHH40N150HV

 $V_{DM} = 1500V$


TO-247HV



G = Gate
A = Anode

K = Cathode
Tab = Anode

Symbol	Test Conditions	Maximum Ratings	
V_{DM}	$T_J = 25^{\circ}C$ to $150^{\circ}C$	1500	V
V_{GK}	Continuous	± 30	V
V_{GK}	Transient	± 40	V
I_{TSM}	$T_C = 25^{\circ}C$, $1\mu s$	7.6	kA
	$T_C = 25^{\circ}C$, $10\mu s$	3.5	kA
P_D	$T_C = 25^{\circ}C$	695	W
T_J		-55 ... +150	$^{\circ}C$
T_{JM}		150	$^{\circ}C$
T_{stg}		-55 ... +150	$^{\circ}C$
T_L	Maximum Lead Temperature for Soldering	300	$^{\circ}C$
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10s	260	$^{\circ}C$
M_d	Mounting Torque	1.13/10	Nm/lb.in
Weight		6	g

Symbol	Test Conditions ($T_J = 25^{\circ}C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
V_{BR}	$I_A = 250\mu A$, $V_{GK} = 0V$	1500		V
$V_{GK(th)}$	$I_A = 250\mu A$, $V_{AK} = V_{GK}$	2.5		5.0 V
V_T	$I_T = 1000A$, $V_{GK} = 15V$		5.95	7.5 V
r_T	$I_T > I_L$, $V_{GK} = 15V$		1.20	m Ω
V_{BO}	$V_{GK} = 15V$		6.45	V
I_D	$V_{AK} = 1500V$, $V_{GK} = 0V$ $T_J = 125^{\circ}C$			15 μA 1 mA
I_L			250	A
I_H			200	A
I_{GKS}	$V_{AK} = 0V$, $V_{GK} = \pm 30V$			± 200 nA

Features

- Very High Voltage Package
- Very High Current Capability

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

- Capacitive Discharge Circuits
- Ignition Circuits
- Solid State Surge Protection

Symbol Test Conditions

($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

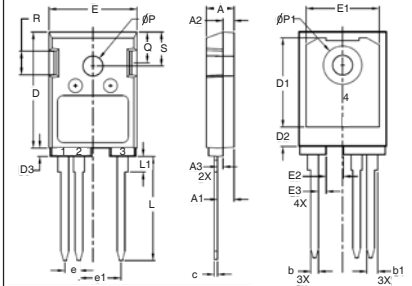
Characteristic Values

	Min.	Typ.	Max.
C_{iks} C_{oks} C_{rks}	$V_{AK} = 25\text{V}, V_{GK} = 0\text{V}, f = 1\text{MHz}$		2825 pF 164 pF 50 pF
$Q_{g(on)}$ Q_{gk} Q_{ga}	$I_C = 40\text{A}, V_{GK} = 15\text{V}, V_{AK} = 600\text{V}$		99 nC 22 nC 36 nC
t_{ri} t_d	Capacitive Discharge, $T_J = 25^\circ\text{C}$ $I_A = 2000\text{A}, V_{GK} = 15\text{V}, R_G = 1\Omega$ $V_{AK} = 1000\text{V}, L < 20\text{nH}$, Notes 2 & 3		100 ns 50 ns
t_{ri} t_d	Capacitive Discharge, $T_J = 125^\circ\text{C}$ $I_A = 2000\text{A}, V_{GK} = 15\text{V}, R_G = 1\Omega$ $V_{AK} = 1000\text{V}, L < 20\text{nH}$, Notes 2 & 3		100 ns 50 ns
R_{thJC} R_{thCS}	0.21		0.18°C/W $^\circ\text{C/W}$

Notes:

1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.
2. It is recommended to use a gate driver capable of supplying more than 4Amps and $\geq 15\text{V}$ gate voltage.
3. Refer to fig. 8 & 9.

TO-247HV Outline



PINS:
1 - Gate 2 - Cathode
3, 4 - Anode

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.114	.122	2.90	3.10
A2	.075	.083	1.90	2.10
A3	.035	.043	0.90	1.10
b	.053	.059	1.35	1.50
b1	.075	.083	1.90	2.10
c	.022	.030	0.55	0.75
D	.819	.843	20.80	21.40
D1	.638	.646	16.20	16.40
D2	.134	.146	3.40	3.70
D3	.055	.063	1.40	1.60
E	.622	.638	15.80	16.20
E1	.520	.528	13.20	13.40
E2	.118	.126	3.00	3.20
E3	.051	.059	1.30	1.50
e	.100	BSC	2.54	BSC
e1	.300	BSC	7.62	BSC
L	.732	.748	18.60	19.00
L1	.106	.118	2.70	3.00
øP	.138	.142	3.50	3.60
øP1	.272	.280	6.90	7.10
Q	.216	.224	5.50	5.70
R	.165	.169	4.20	4.30
S	.240	.248	6.10	6.30

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2
by one or more of the following U.S. patents: 4,860,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

Fig. 1. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

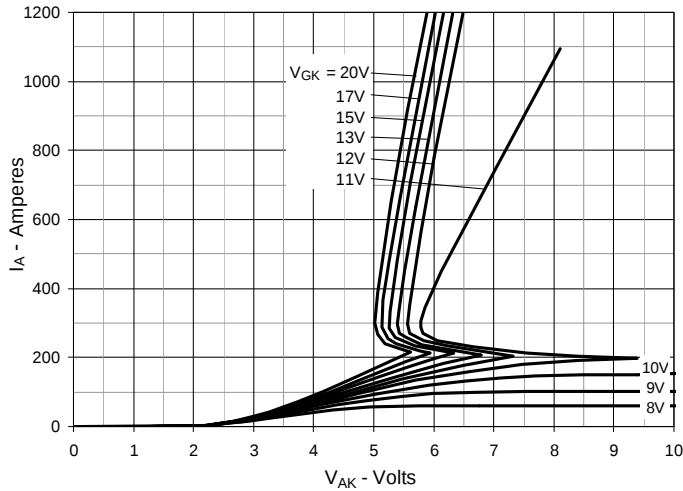


Fig. 2. Extended Output Characteristics @ $T_J = 125^\circ\text{C}$

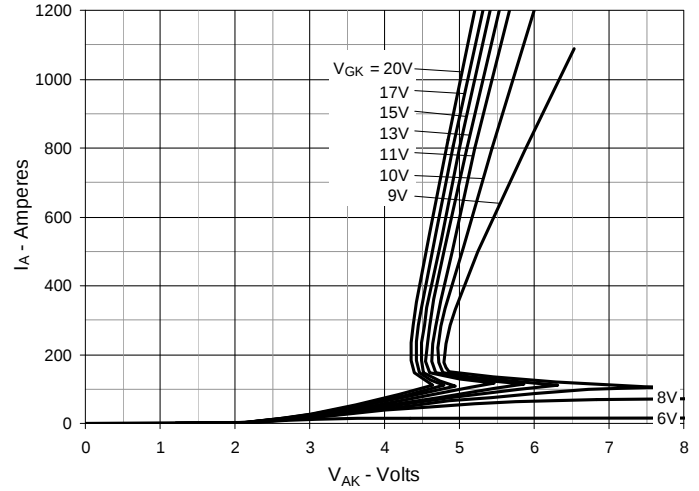


Fig. 3. Extended Output Characteristics @ $T_J = -40^\circ\text{C}$

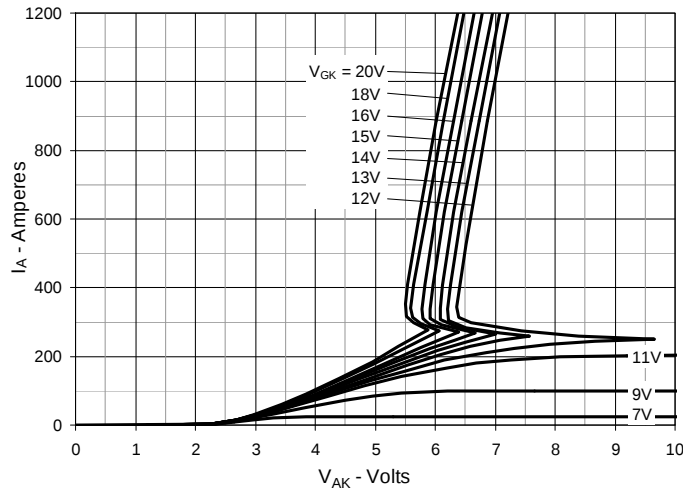


Fig. 4. Gate Charge

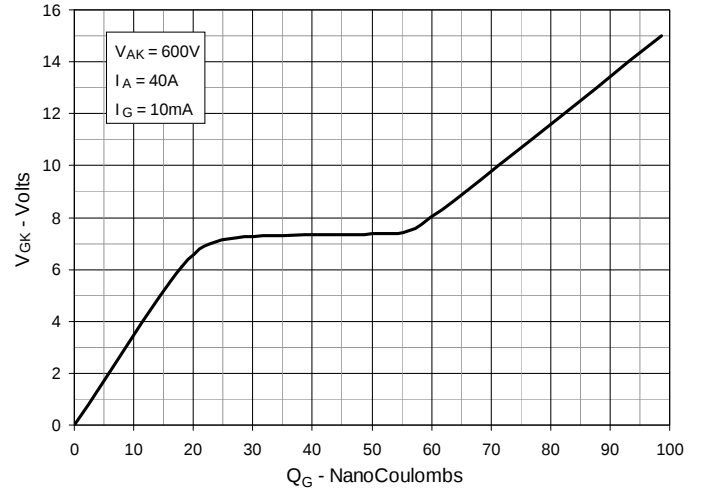


Fig. 5. Capacitance

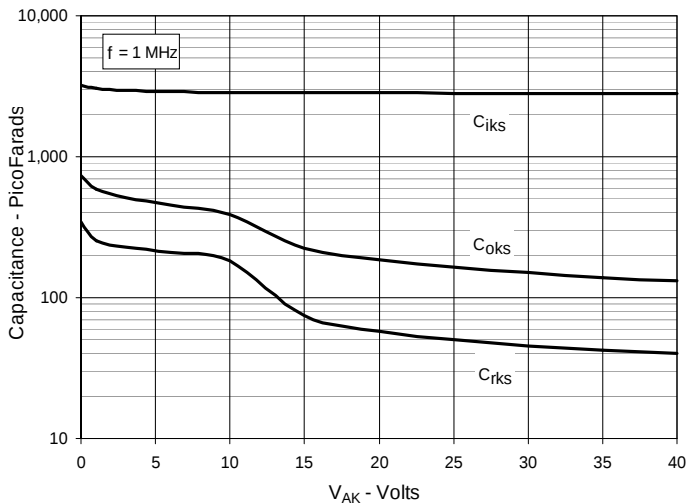
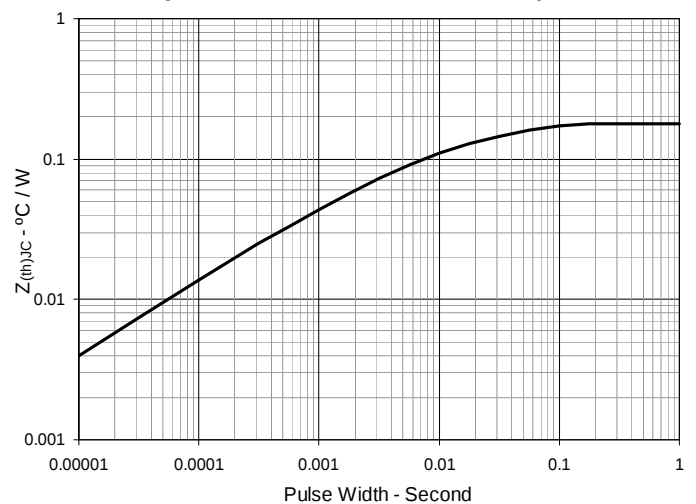


Fig. 6. Maximum Transient Thermal Impedance



The diagram shows a ladder network. On the left, a voltage source is connected in series with a resistor R_1 . This is followed by a shunt capacitor C_1 . Then, a resistor R_2 is in series, followed by a shunt capacitor C_2 . This pattern continues with a resistor R_3 and a shunt capacitor C_3 . The network continues with ellipses, and the output is labeled i .

i	Ri (Ω)	Ci (F)
1	0.015004	0.005397
2	0.071079	0.028026
3	0.051007	0.121930
4	0.002310	2.500000

[illegible]

A graph showing the switching transition of a MOSFET. The vertical axis represents both drain-source voltage (V_{AK}) and drain current (I_A). The horizontal axis represents Time. The V_{AK} curve starts at a high level and falls to zero. The I_A curve starts at zero and rises to a peak. A vertical dashed line marks the time when V_{AK} is at 90% of its initial value and I_A is at 10% of its peak value. The time interval between the 10% and 90% points of the I_A curve is labeled $tr1$.



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