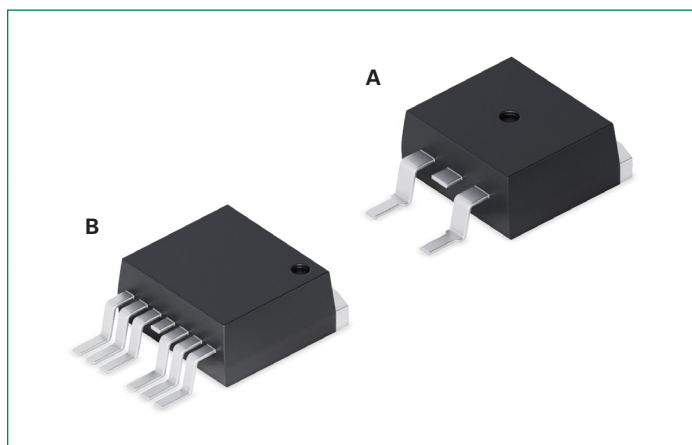


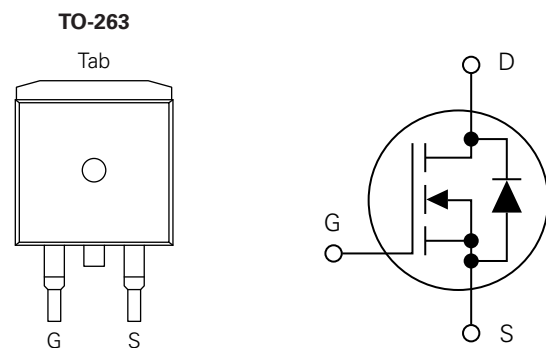
IXTA130N15X4 IXTA130N15X4-7

150 V, 8.0 m Ω X4-Class Power MOSFET™



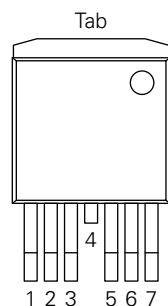
A: TO-263, B: TO-263 (7 Leads)

Pinout Diagram



G: Gate; D: Drain; S: Source;
Tab: Drain

TO-263 (7-Leads)



1: Gate; 2, 3, 5, 6, 7: Source;
4 (Tab): Drain

Features:

- International Standard Packages
- Avalanche Rated
- Low Package Inductance
- Low $R_{DS(ON)}$ and Q_G

Advantages:

- High Power Density
- Easy to Mount
- Space Savings

Applications:

- Switch-Mode and Resonant-Mode
- Power Supplies
- DC-DC Converters
- PFC Circuits
- AC and DC Motor Drives
- Robotics and Servo Controls

Product Summary

Characteristic	Value	Unit
V_{DSS}	150	V
I_{D25}	130	A
$R_{DS(on)}$	≤ 8.0	m Ω

Maximum Ratings

Symbol	Characteristics	Conditions	Value	Units
V_{DSS}	Drain-Source Voltage	$T_J = 25^{\circ}\text{C}$ to 175°C	150	V
V_{DGR}	Drain-Gate Voltage	$T_J = 25^{\circ}\text{C}$ to 175°C , $R_{GS} = 1\text{ M}\Omega$	150	V
V_{GSS}	Gate-Source Voltage	Continuous	± 20	V
V_{GSM}		Transient	± 30	
I_{D25}	Drain Current	$T_C = 25^{\circ}\text{C}$	130	A
$I_{L(RMS)}$	External Lead Current Limit	–	120	
I_{DM}	Peak Drain Current	$T_C = 25^{\circ}\text{C}$, Pulse width limited by T_{JM}	210	
I_A	Avalanche Current	$T_C = 25^{\circ}\text{C}$	65	A
E_{AS}	Avalanche Energy	$T_C = 25^{\circ}\text{C}$	800	mJ
dv/dt	Reverse Diode dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^{\circ}\text{C}$	50	V/ns
P_D	Power Dissipation	$T_C = 25^{\circ}\text{C}$	480	W
T_J	Operating Junction Temperature	–	-55 to +175	$^{\circ}\text{C}$
T_{JM}	Maximum Junction Temperature	–	175	
T_{stg}	Storage Temperature	–	-55 to +175	
T_{SOLD}	Soldering Temperature	Plastic Body for 10 s	260	$^{\circ}\text{C}$
F_C	Mounting Force	–	10..65 / 2.2..14.6	N/lb
W	Weight	TO-263	2.5	g
		TO-263 (7-Leads)	3.0	

Thermal Characteristics

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$R_{th, JC}$	Thermal Resistance, junction-to-case	–	–	0.31	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics – Static ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	150	–	–	V
$V_{GS(th)}$	Gate Threshold Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{DS} = V_{GS}$	2.5	–	4.5	V
I_{GSS}	Gate-Source Leakage Current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	–	–	± 100	nA
I_{DSS}	Drain-Source Current	$V_{DS} = V_{DSS}$, $V_{GS} = 0\text{ V}$	–	–	5	μA
		$V_{DS} = V_{DSS}$, $V_{GS} = 0\text{ V}$, $T_J = 125^{\circ}\text{C}$	–	–	200	μA
$R_{DS(on)}$	Drain-Source On-Resistance ¹	$V_{GS} = 10\text{ V}$, $I_D = 0.5 \times I_{D25}$	–	7.0	8.5	m Ω

Note 1: Pulse test, $t \leq 300\text{ }\mu\text{s}$, duty cycle, $d \leq 2\%$

Electrical Characteristics – Dynamic ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
g_{fs}	Transconductance ¹	$V_{DS} = 10\text{ V}, I_D = 60\text{ A}$	70	120	–	S
R_{Gi}	Gate Input Resistance	–	–	3.4	–	Ω
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	–	4770	–	pF
C_{oss}	Output Capacitance		–	710	–	pF
C_{rss}	Reverse Transfer Capacitance		–	3.5	–	pF
$C_{o(er)}$	Effective Output Capacitance – Energy Related	$V_{GS} = 0\text{ V}, V_{DS} = 0.8 \times V_{DSS}$	–	560	–	pF
$C_{o(tr)}$	Effective Output Capacitance – Time Related		–	1850	–	pF
$Q_{g(on)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \times V_{DSS},$ $I_D = 0.5 \times I_{D25}$	–	87	–	nC
Q_{gs}	Gate-Source Charge		–	24	–	
Q_{gd}	Gate-Drain Charge		–	23	–	
$t_{d(on)}$	Turn-on Delay Time	Resistive Switching $V_{GS} = 10\text{ V}, V_{DS} = 0.5 \times V_{DSS},$ $I_D = 0.5 \times I_{D25}, R_{G(ext)} = 5\ \Omega$	–	20	–	ns
t_r	Rise Time		–	27	–	
$t_{d(off)}$	Turn-off Delay Time		–	100	–	
t_f	Fall Time		–	10	–	

Source-Drain Diode Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
I_S	Continuous Diode Forward Current	$V_{GS} = 0\text{ V}$	–	–	130	A
I_{SM}	Diode Pulse Current	Repetitive, Pulse width limited by T_{JM}	–	–	520	A
V_{SD}	Diode Forward Voltage ¹	$I_F = 100\text{ A}, V_{GS} = 0\text{ V}$	–	–	1.4	V
t_{rr}	Reverse Recovery Time	$I_F = 65\text{ A}, -di/dt = 100\text{ A}/\mu\text{s},$ $V_R = 75\text{ V}$	–	93	–	ns
I_{rm}	Reverse Recovery Charge		–	6.7	–	A
Q_{rm}	Reverse Recovery Current		–	310	–	nC

Note 1: Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle, $d \leq 2\%$

Characteristic Curves

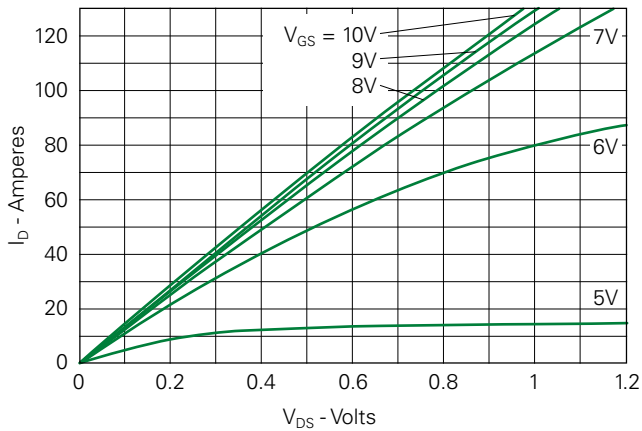
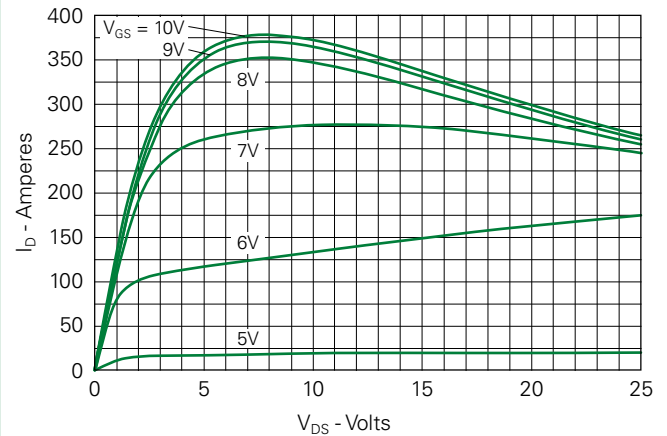
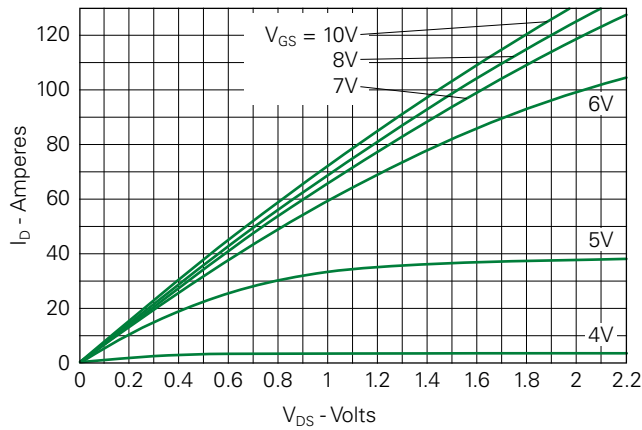
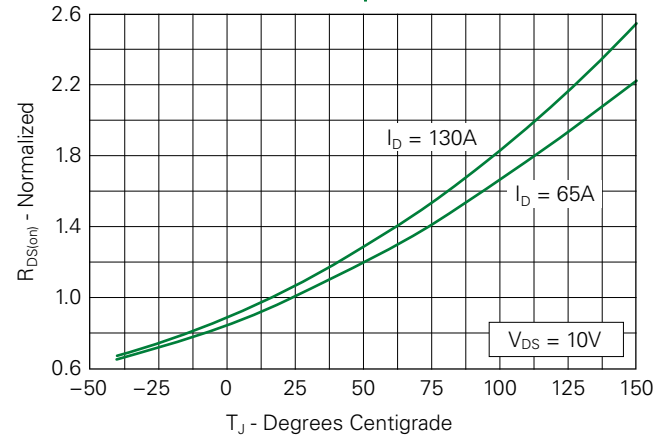
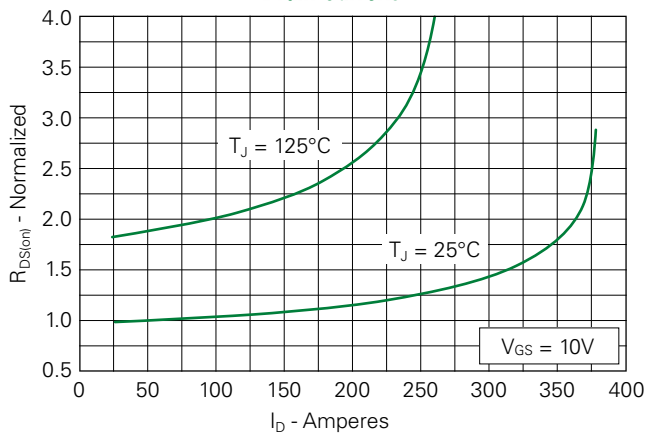
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$ Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$ Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$ Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 65\text{A}$ Value vs. Junction TemperatureFig. 5. $R_{DS(on)}$ Normalized to $I_D = 65\text{A}$ Value vs. Drain Current

Fig. 6. Normalized Breakdown & Threshold Voltages vs. Junction Temperature

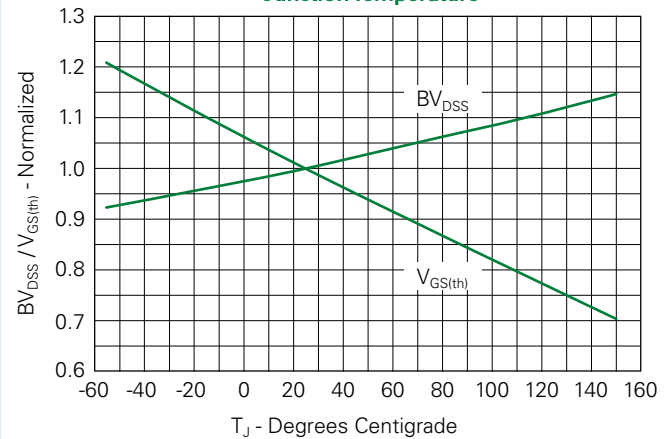


Fig. 7. Maximum Drain Current vs. Case Temperature

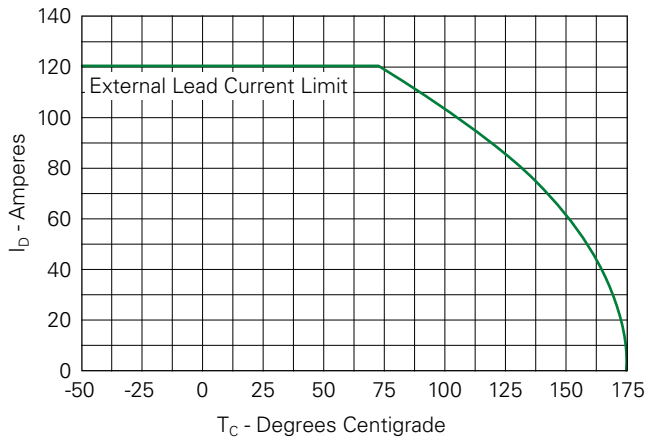


Fig. 8. Input Admittance

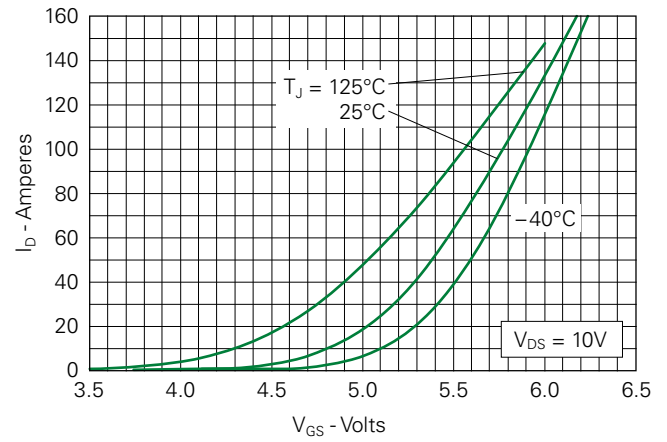


Fig. 9. Transconductance

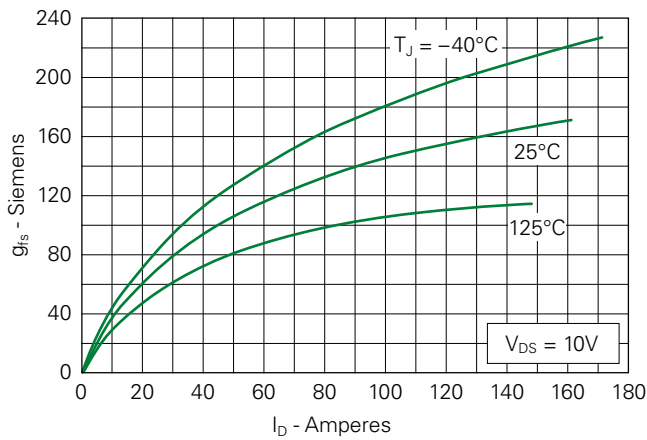


Fig. 10. Forward Voltage Drop of Intrinsic Diode

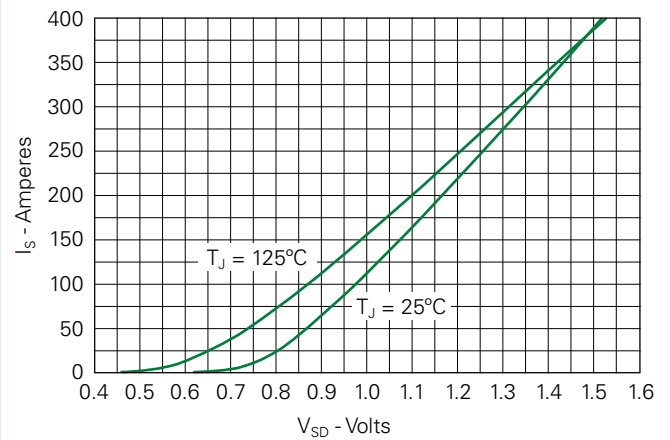


Fig. 11. Gate Charge

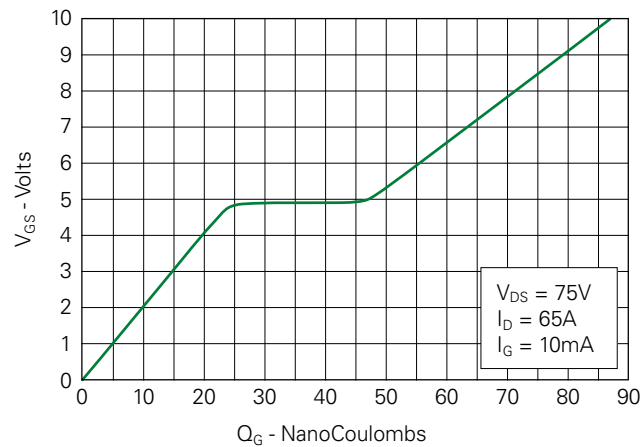


Fig. 12. Capacitance

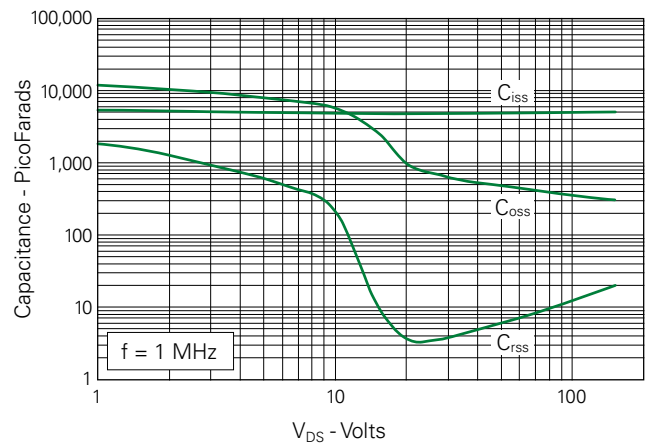


Fig. 13. Output Capacitance Stored Energy

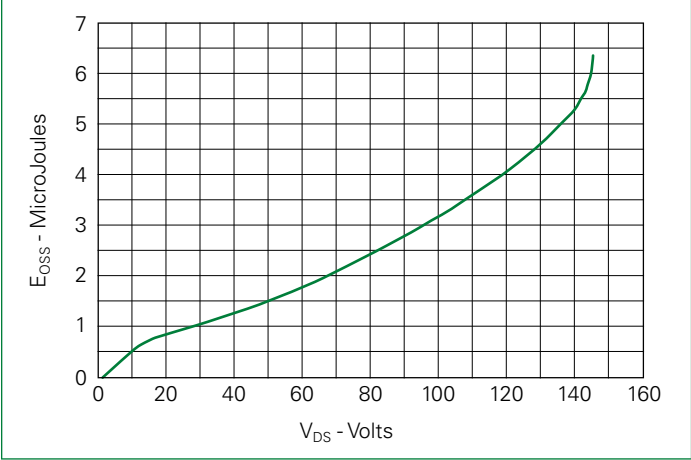


Fig. 14. Forward-Bias Safe Operating Area

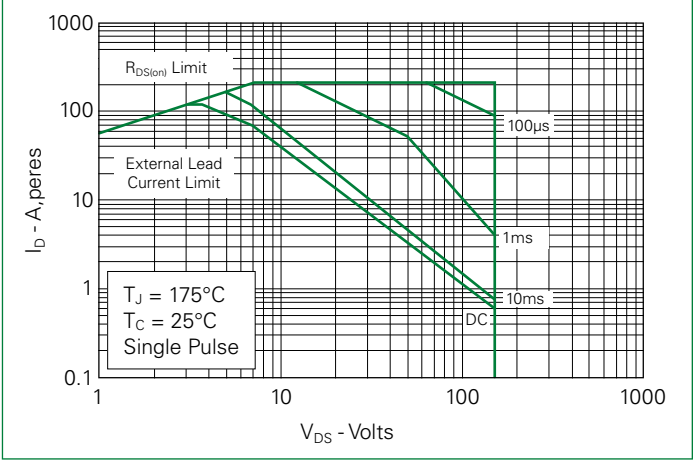
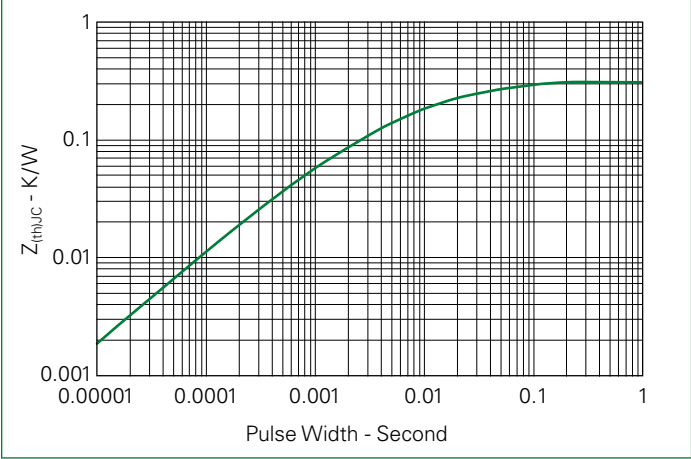
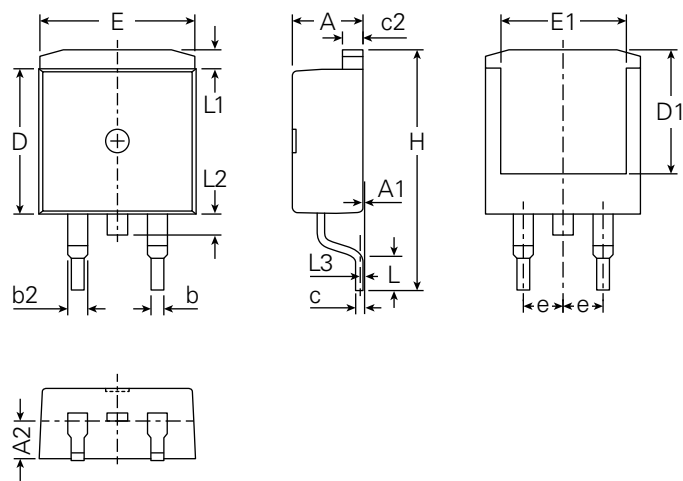


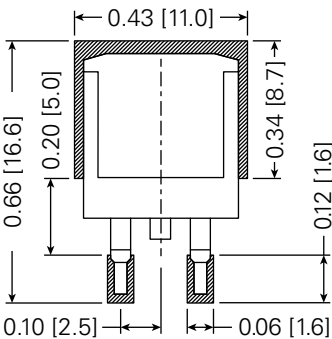
Fig. 15. Maximum Transient Thermal Impedance



Part Outline Drawing (TO-263)

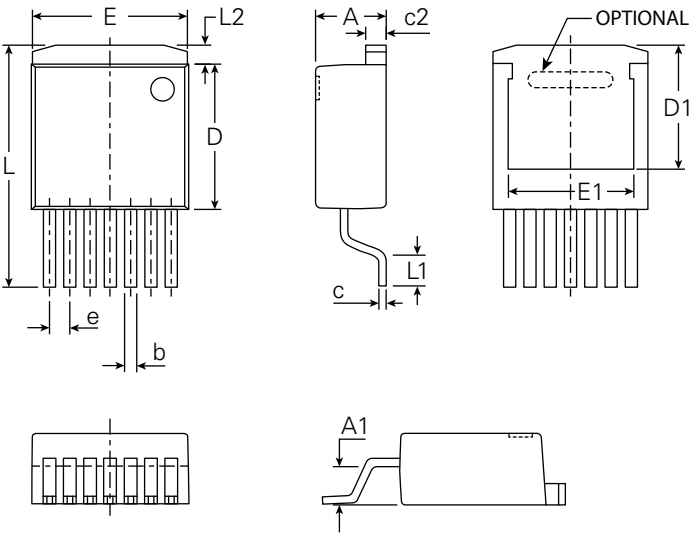


Symbol	Inches			Millimeters		
	Min.	Typical	Max.	Min.	Typical	Max
A	0.170	–	0.185	4.30	–	4.70
A1	0.000	–	0.008	0.00	–	0.20
A2	0.091	–	0.098	2.30	–	2.50
b	0.028	–	0.035	0.70	–	0.90
b2	0.046	–	0.060	1.18	–	1.52
c	0.018	–	0.024	0.45	–	0.60
c2	0.049	–	0.060	1.25	–	1.52
D	0.340	–	0.370	8.63	–	9.40
D1	0.300	–	0.327	7.62	–	8.30
E	0.380	–	0.410	9.65	–	10.41
E1	0.270	–	0.330	6.86	–	8.38
e	0.100 BSC			2.54 BSC		
H	0.580	–	0.620	14.73	–	15.75
L	0.075	–	0.105	1.91	–	2.67
L1	0.039	–	0.060	1.00	–	1.52
L2	–	–	0.070	–	–	1.77
L3	0.010 BSC			0.254 BSC		

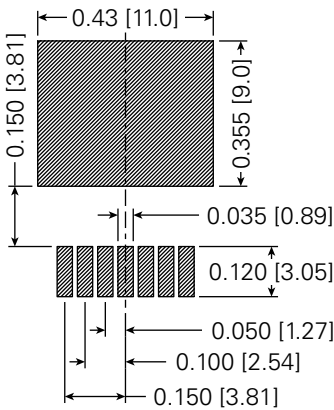


Minimum PCB Footprint Layout

Part Outline Drawing (TO-263 7-Leads)



Symbol	Inches			Millimeters		
	Min.	Typical	Max.	Min.	Typical	Max
A	0.170	–	0.185	4.30	–	4.70
A1	0.085	–	0.104	2.15	–	2.65
b	0.026	–	0.035	0.65	–	0.90
c	0.016	–	0.024	0.40	–	0.60
c2	0.049	–	0.055	1.25	–	1.40
D	0.355	–	0.370	9.00	–	9.40
D1	0.263	–	0.271	6.70	–	6.90
E	0.386	–	0.402	9.80	–	10.20
E1	0.326	–	0.335	8.30	–	8.50
e	0.050 BSC			1.27 BSC		
L	0.591	–	0.614	15.00	–	15.60
L1	0.091	–	0.110	2.30	–	2.80
L2	0.039	–	0.059	1.00	–	1.50



Recommended Minimum Footprint for SMD

Disclaimer Notice

Information furnished is believed to be accurate and reliable. However, users should independently evaluate the suitability of and test each product selected for their own applications. Littelfuse products are not designed for, and may not be used in, all applications. Read complete Disclaimer Notice at <http://www.littelfuse.com/disclaimer-electronics>.



Part of:

