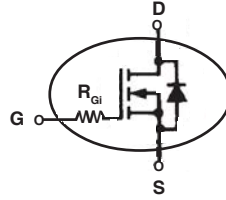


LinearL2™ Power MOSFET w/ Extended FBSOA

IXTK80N30L2 IXTX80N30L2

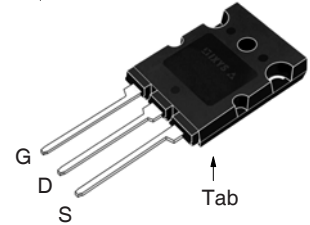
N-Channel Enhancement Mode
Avalanche Rated



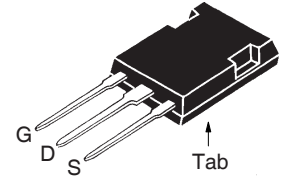
$$\begin{aligned} V_{DSS} &= 300V \\ I_{D25} &= 80A \\ R_{DS(on)} &\leq 38m\Omega \end{aligned}$$

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	300	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1M\Omega$	300	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	80	A
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	200	A
I_A	$T_C = 25^\circ\text{C}$	80	A
E_{AS}	$T_C = 25^\circ\text{C}$	3	J
P_D	$T_C = 25^\circ\text{C}$	960	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ\text{C}$
M_d	Mounting Torque (TO-264)	1.13/10	Nm/lb.in
F_C	Mounting Force (PLUS247)	20..120 / 4.5..27	N/lb
Weight	TO-264	10	g
	PLUS247	6	g

TO-264 (IXTK)



PLUS247 (IXTX)



G = Gate D = Drain
S = Source Tab = Drain

Features

- Designed for Linear Operation
- International Standard Packages
- Avalanche Rated
- Guaranteed FBSOA at 75°C

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- Solid State Circuit Breakers
- Soft Start Controls
- Linear Amplifiers
- Programmable Loads
- Current Regulators

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 1mA$	300		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 3mA$	2.5		4.5 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ\text{C}$			10 μA 250 μA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1	30		38 m Ω

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10V, I_D = 0.5 \cdot I_{D25}$, Note 1	24	36	48
C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		19.1	nF
C_{oss}			1760	pF
C_{rss}			490	pF
R_{Gi}	Integrated Gate Input Resistor		0.88	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10V, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ $R_G = 1\Omega$ (External)		40	ns
t_r			180	ns
$t_{d(off)}$			174	ns
t_f			67	ns
$Q_{g(on)}$	$V_{GS} = 10V, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$		660	nC
Q_{gs}			107	nC
Q_{gd}			364	nC
R_{thJC}			0.15	$^{\circ}C/W$
R_{thCS}				$^{\circ}C/W$

Safe Operating Area Specification

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
SOA	$V_{DS} = 300V, I_D = 1.9A, T_C = 75^{\circ}C, T_p = 5s$	570		W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0V$			80
I_{SM}	Repetitive, pulse Width Limited by T_{JM}			320
V_{SD}	$I_F = I_S, V_{GS} = 0V$, Note 1			1.4
t_{rr}	$I_F = 40A, -di/dt = 100A/\mu s$ $V_R = 100V$		485	ns
Q_{RM}			10	μC
I_{RM}			42	A

Note 1. Pulse test, $t \leq 300\mu s$, duty cycle, $d \leq 2\%$.

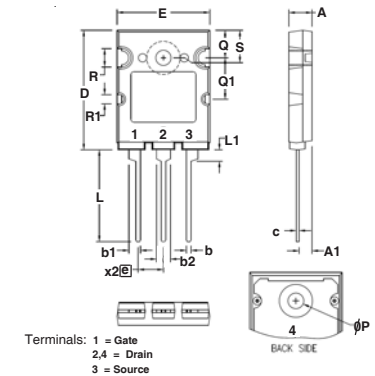
ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

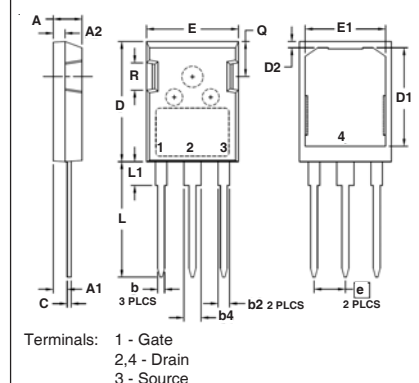
IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065B1	6,683,344	6,727,585	7,005,734B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123B1	6,534,343	6,710,405B2	6,759,692	7,063,975B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728B1	6,583,505	6,710,463	6,771,478B2	7,071,537	

TO-264 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.70	5.30
A1	.102	.118	2.60	3.00
b	.035	.049	0.90	1.25
b1	.091	.106	2.30	2.70
b2	.110	.126	2.80	3.20
c	.020	.033	0.50	0.85
D	1.012	1.035	25.70	26.30
E	.776	.799	19.70	20.30
e	.215 BSC		5.46 BSC	
L	.768	.807	19.50	20.50
L1	.091	.106	2.30	2.70
ϕP	.122	.138	3.10	3.50
Q	.228	.244	5.80	6.20
Q1	.346	.362	8.80	9.20
ϕR	.150	.165	3.80	4.20
$\phi R1$	.071	.087	1.80	2.20
S	.228	.244	5.80	6.20

PLUS 247™ Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.087	1.91	2.20
b4	.115	.126	2.92	3.20
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
D1	.650	.690	16.51	17.53
D2	.035	.050	0.89	1.27
E	.620	.635	15.75	16.13
E1	.520	.560	13.08	14.22
e	.215 BSC		5.45 BSC	
L	.780	.810	19.81	20.57
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

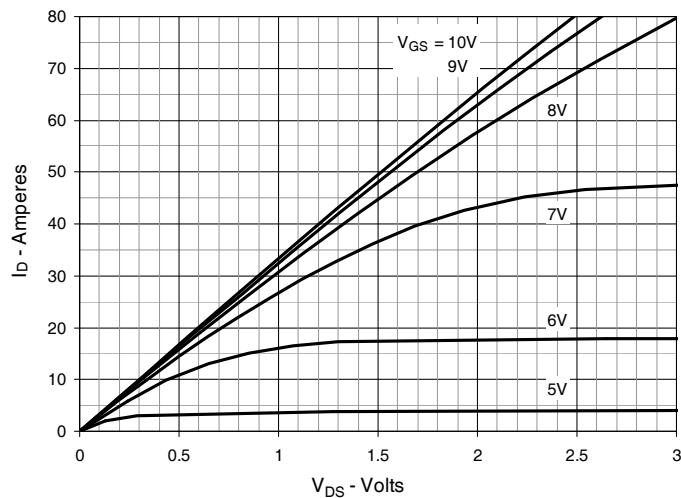


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

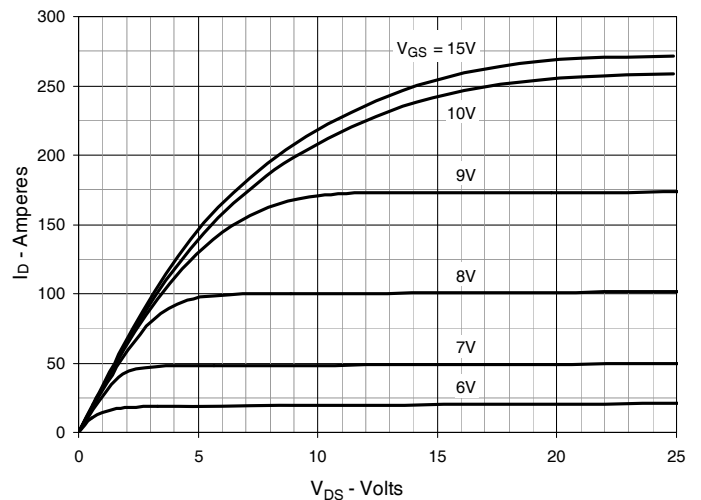


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

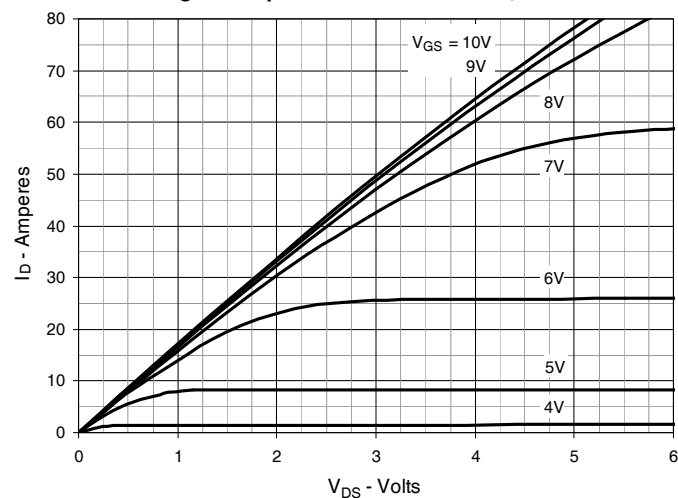


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 40\text{A}$ Value vs. Junction Temperature

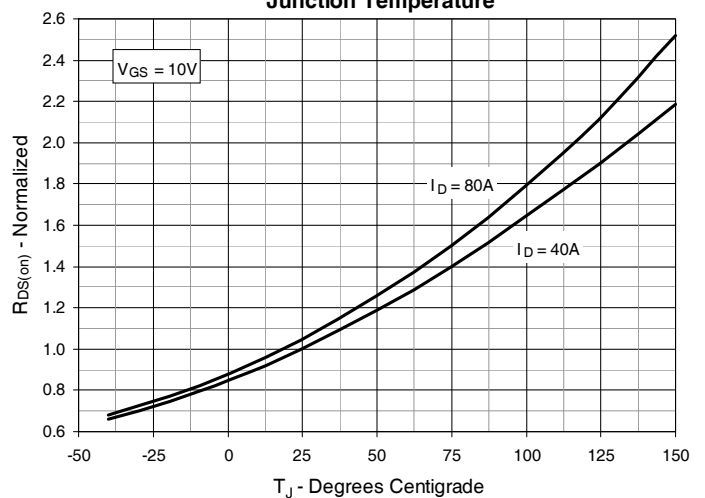


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 40\text{A}$ Value vs. Drain Current

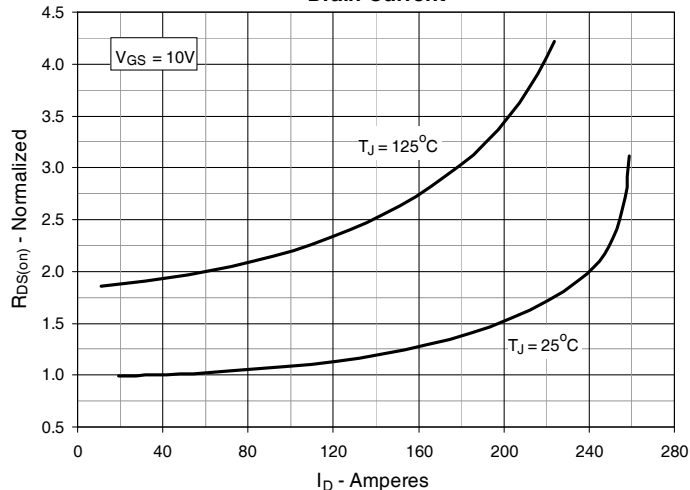


Fig. 6. Normalized Breakdown & Threshold Voltages vs. Junction Temperature

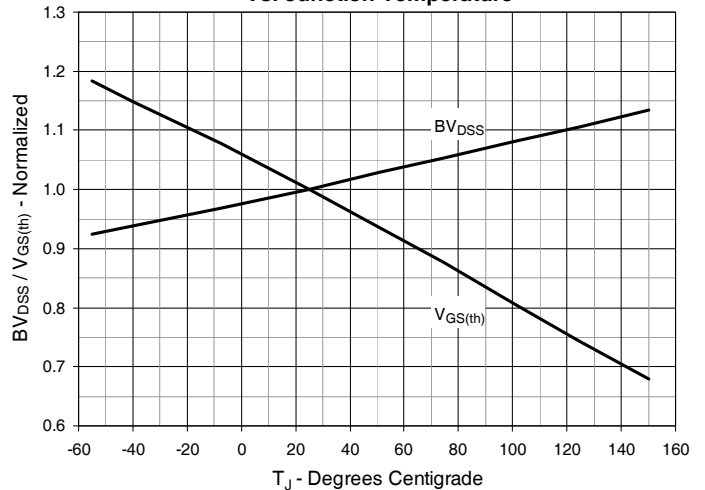


Fig. 7. Maximum Drain Current vs. Case Temperature

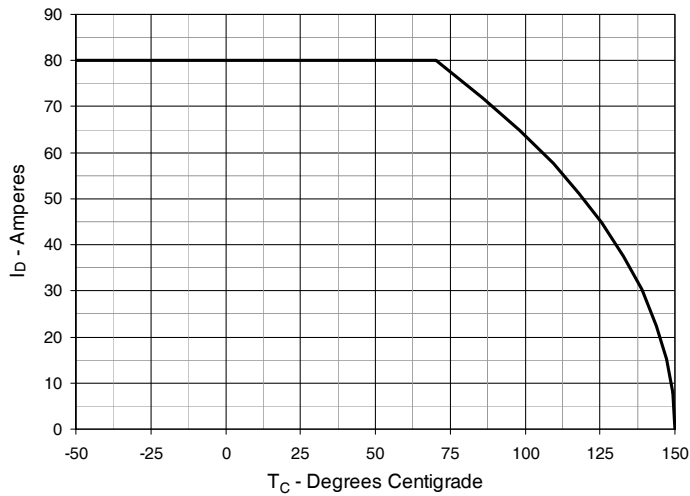


Fig. 8. Input Admittance

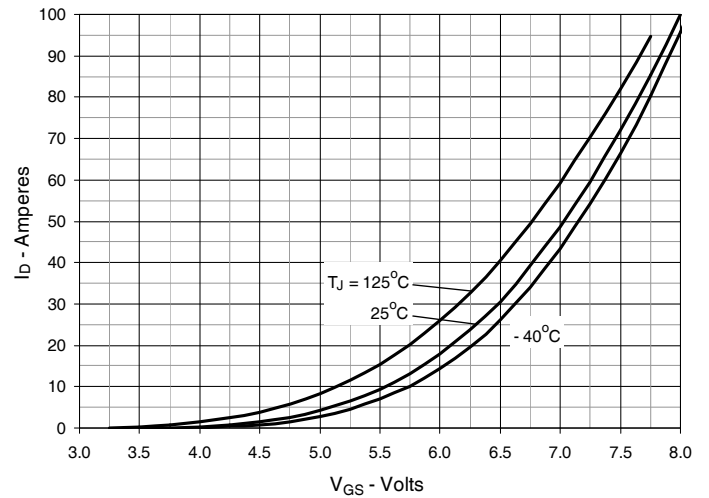


Fig. 9. Transconductance

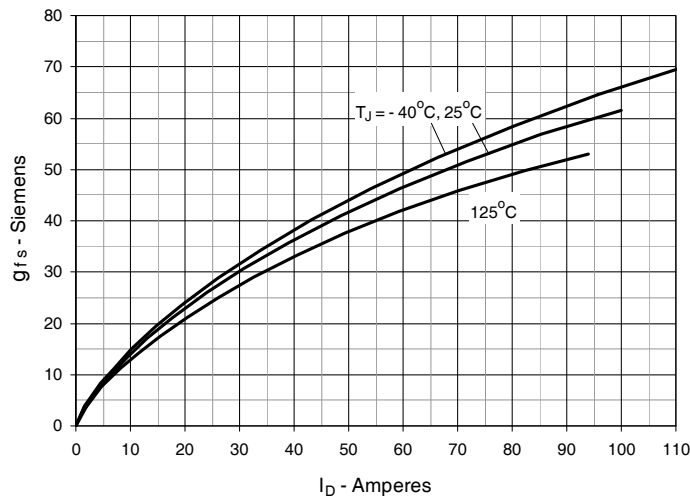


Fig. 10. Forward Voltage Drop of Intrinsic Diode

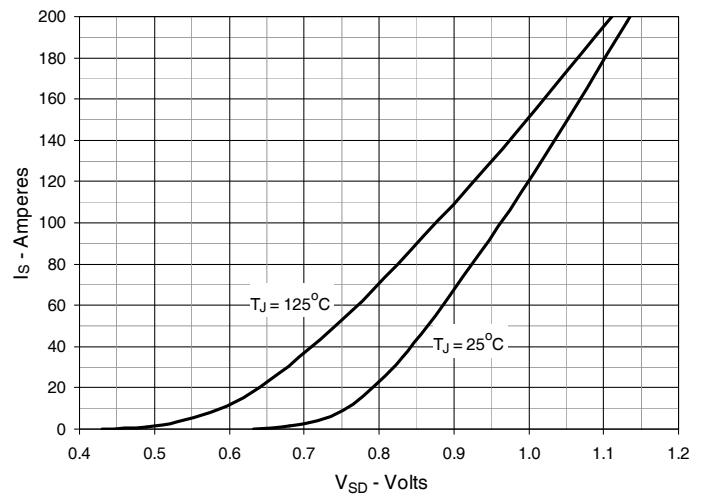


Fig. 11. Gate Charge

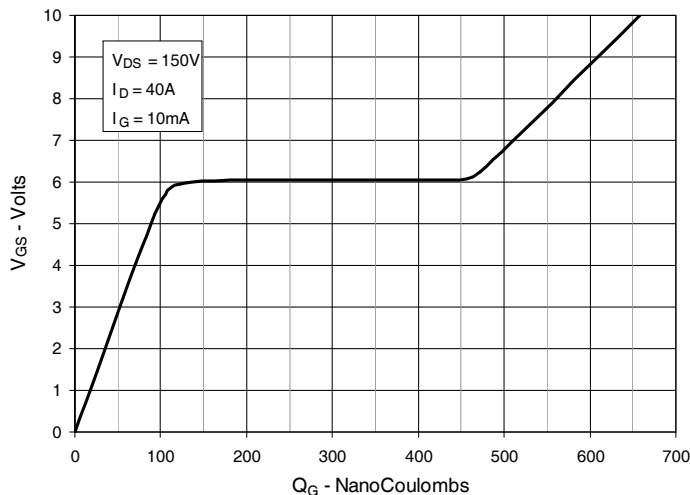


Fig. 12. Capacitance

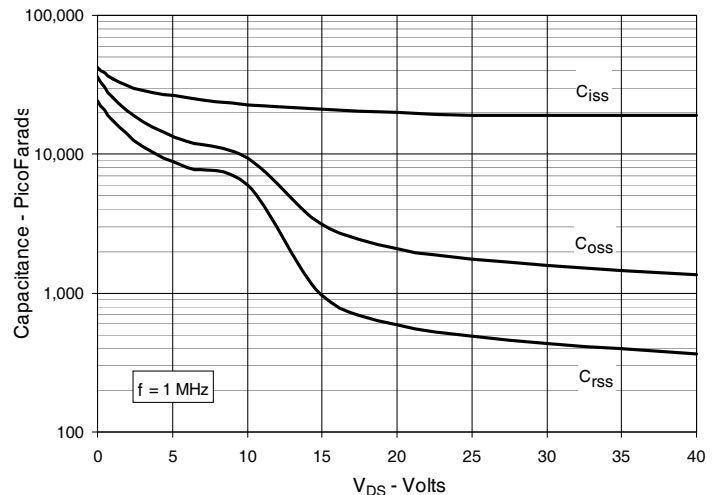


Fig. 13. Forward-Bias Safe Operating Area

@ $T_C = 25^\circ\text{C}$

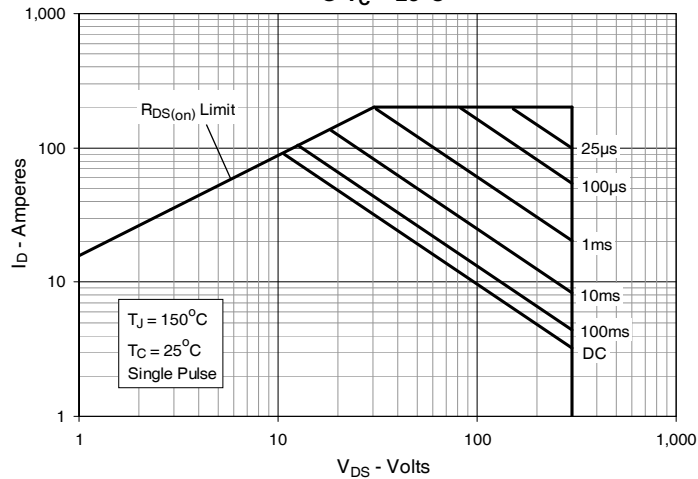


Fig. 14. Forward-Bias Safe Operating Area

@ $T_C = 75^\circ\text{C}$

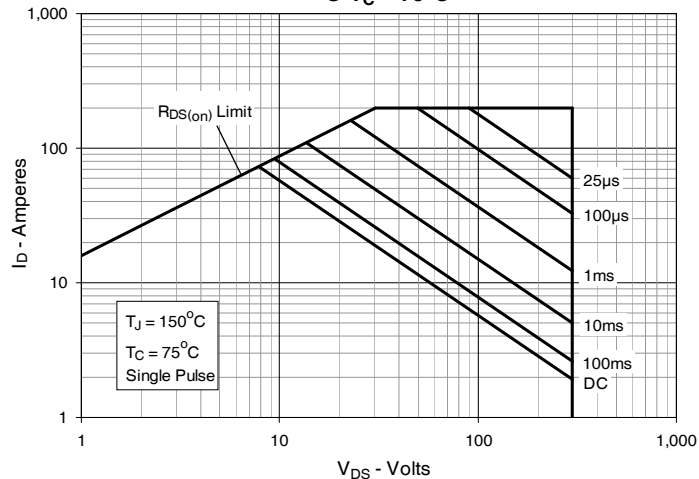
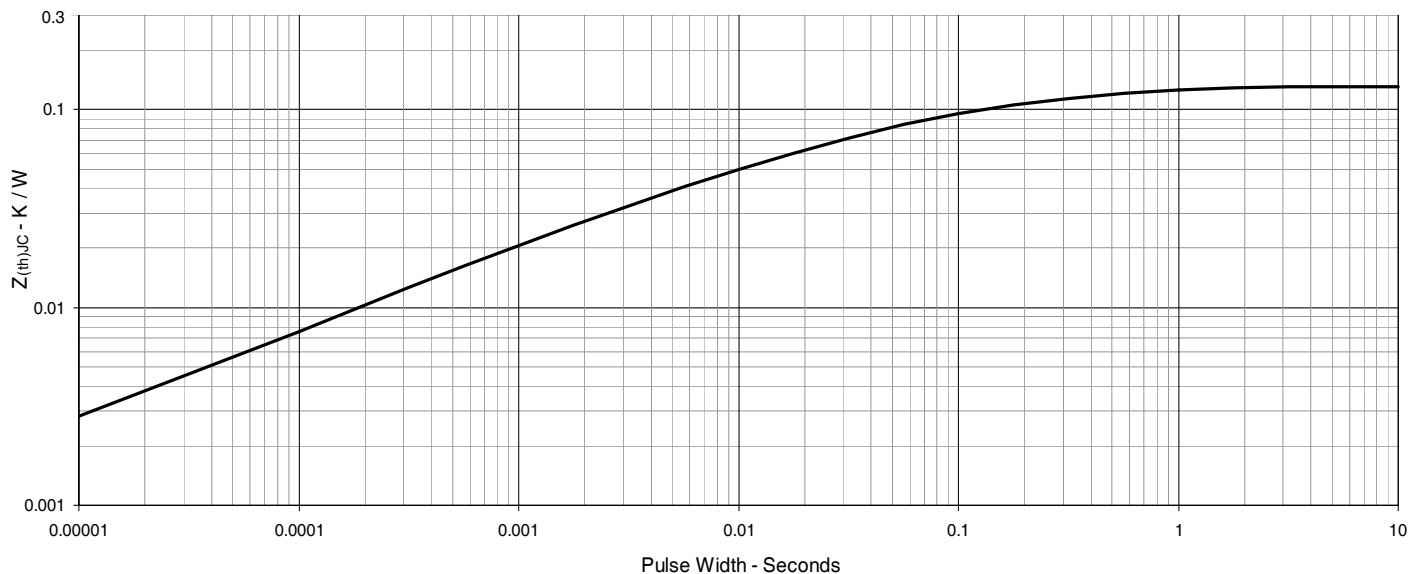


Fig. 15. Maximum Transient Thermal Impedance





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