IXYS

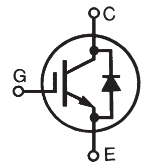
High Voltage, High Gain BiMOSFET™

IXBL64N250

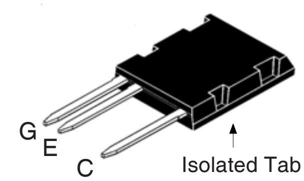
V_{CES} = 2500V
I_{C110} = 46A
$V_{CE(sat)}$ ≤ 3.0V

Monolithic Bipolar MOS Transistor

(Electrically Isolated Tab)



ISOPLUS i5-Pak™



G = Gate C = Collector
E = Emitter

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	2500	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	2500	V
V_{GES}	Continuous	±25	V
V_{GEM}	Transient	±35	V
I_{C25}	T_C = 25°C	116	A
I_{C110}	T_C = 110°C	46	A
I_{CM}	T_C = 25°C, 1ms	750	A
SSOA	V_{GE}= 15V, T_{VJ} = 125°C, R_G = 1Ω	I_{CM} = 160	A
(RBSOA)	Clamped Inductive Load	V_{CE} ≤ 0.8 • V_{CES}	
T_{SC} **(SCSOA)**	V_{GE} = 15V, T_J = 125°C, R_G = 5Ω, V_{CE} = 1250V, Non-Repetitive	10	μs
P_C	T_C = 25°C	500	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10	260	°C
V_{ISOL}	50/60Hz, 1 minute	2500	V~
F_C	Mounting Force with Clip	30..170 / 7..36	Nm/lb-in.
Weight		8	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 1mA, V_{GE} = 0V	2500			V
$V_{GE(th)}$	I_C = 4mA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = 0.8 • V_{CES}, V_{GE} = 0V			50	μA
	Note 2, T_J = 125°C			6	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 25V			±200	nA
$V_{CE(sat)}$	I_C = 64A, V_{GE} = 15V, Note 1		2.5	3.0	V
	T_J = 125°C		3.1		V

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V~ Electrical Isolation
- High Blocking Voltage
- Low Switching Losses
- High Current Handling Capability
- Anti-Parallel Diode

Advantages

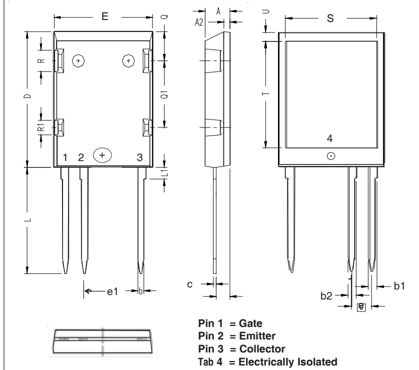
- High Power Density
- Low Gate Drive Requirement

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Uninterrupted Power Supplies (UPS)
- Capacitor Discharge Circuits
- Laser Generators

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fS}	I_C = 64A, V_{CE} = 10V, Note 1	40	72		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		8900		pF
C_{oes}			345		pF
C_{res}			118		pF
Q_g	I_C = 64A, V_{GE} = 15V, V_{CE} = 600V		400		nC
Q_{ge}			46		nC
Q_{gc}			155		nC
$t_{d(on)}$	**Resistive Switching Times, T_J = 25°C**		49		ns
t_r	I_C = 128A, V_{GE} = 15V		318		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 1Ω		232		ns
t_f			170		ns
$t_{d(on)}$	**Resistive Switching Times, T_J = 125°C**		54		ns
t_r	I_C = 128A, V_{GE} = 15V		578		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 1Ω		222		ns
t_f			175		ns
R_{thJC}				0.25	°C/W
R_{thCS}			0.15		°C/W

ISOPLUS i5-Pak™ HV (IXBL) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.190	0.205	4.83	5.21
A1	0.102	0.118	2.59	3.00
A2	0.046	0.055	1.17	1.40
b	0.045	0.055	1.14	1.40
b1	0.063	0.072	1.60	1.83
b2	0.058	0.068	1.47	1.73
c	0.020	0.029	0.51	0.74
D	1.020	1.040	25.91	26.42
E	0.770	0.799	19.56	20.29
e	0.150 BSC		3.81 BSC	
e1	0.450 BSC		11.43 BSC	
L	0.780	0.820	19.81	20.83
L1	0.080	0.102	2.03	2.59
Q	0.210	0.235	5.33	5.97
Q1	0.490	0.513	12.45	13.03
R	0.150	0.180	3.81	4.57
R1	0.100	0.130	2.54	3.30
S	0.668	0.690	16.97	17.53
T	0.801	0.821	20.34	20.85
U	0.065	0.080	1.65	2.03

Reverse Diode

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
V_F	I_F = 64A, V_{GE} = 0V, Note 1			3.0	V
t_{rr}	I_F = 64A, V_{GE} = 0V, $-di_F/dt$ = 650A/μs		160		ns
I_{RM}	V_R = 600V, V_{GE} = 0V		480		A

Notes:

1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Part must be heatsunk for high-temp Ices measurement.

Additional provisions for lead-to-lead isolation are required at V_{CE} >1200V.

Fig. 1. Output Characteristics @ $T_J = 25^oC$

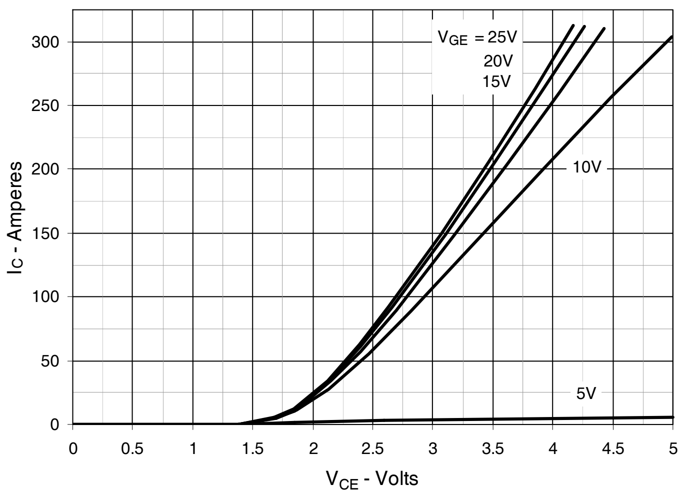


Fig. 2. Output Characteristics @ $T_J = 125^oC$

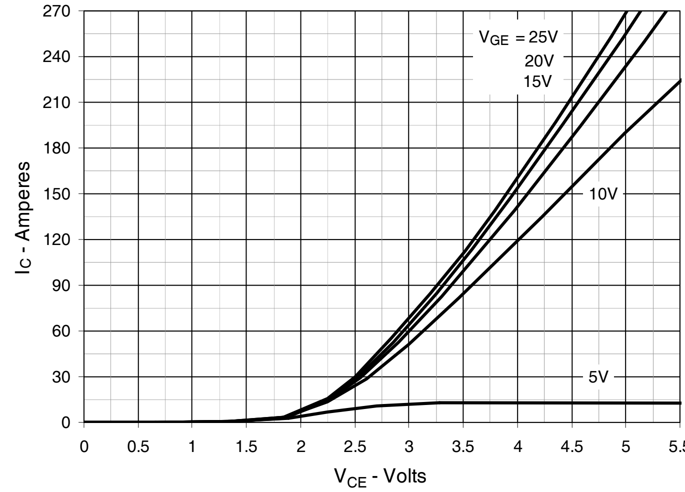


Fig. 3. Dependence of $V_{CE(sat)}$ on Junction Temperature

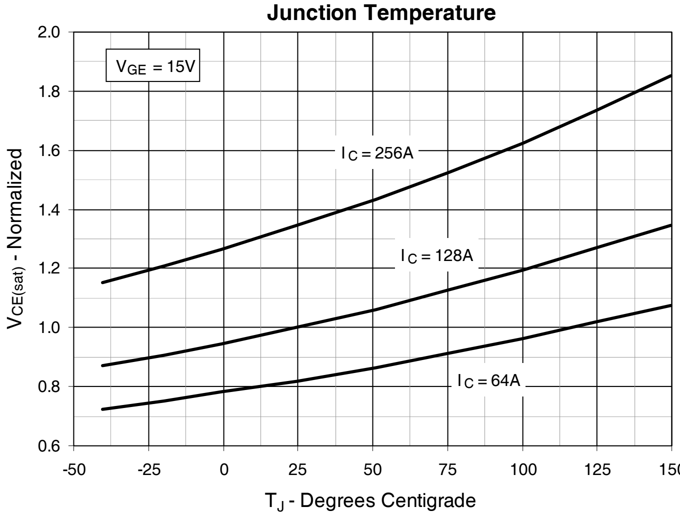


Fig. 4. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

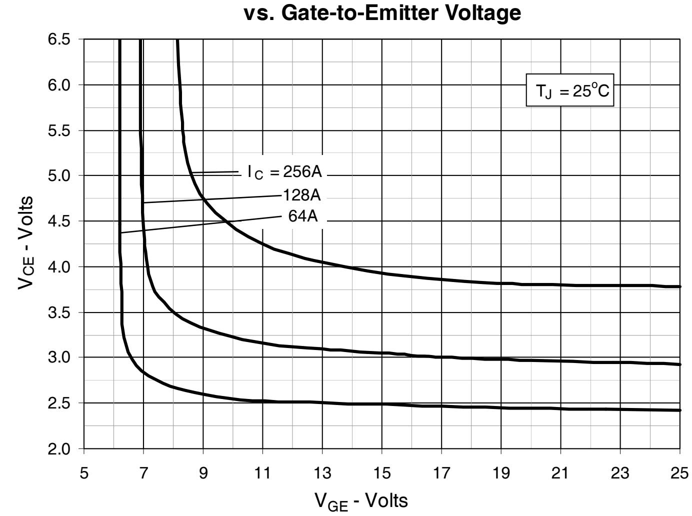


Fig. 5. Breakdown & Threshold Voltages vs. Junction Temperature

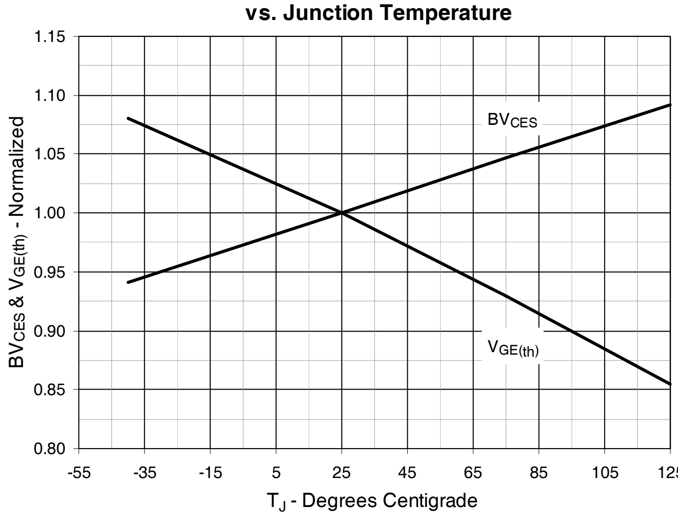


Fig. 6. Input Admittance

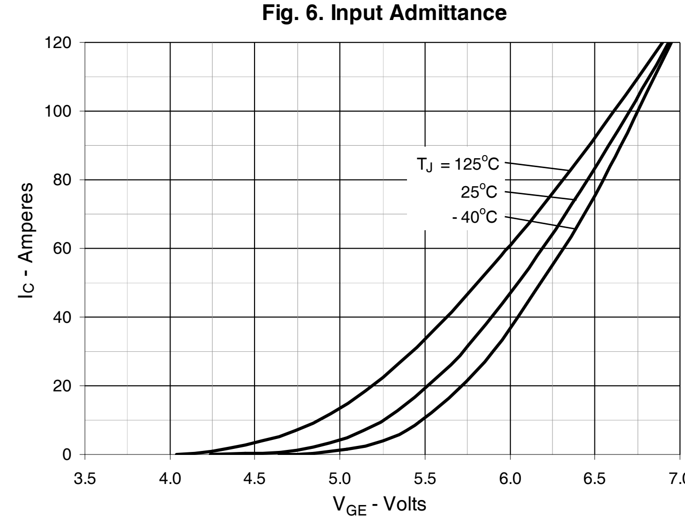


Fig. 7. Transconductance

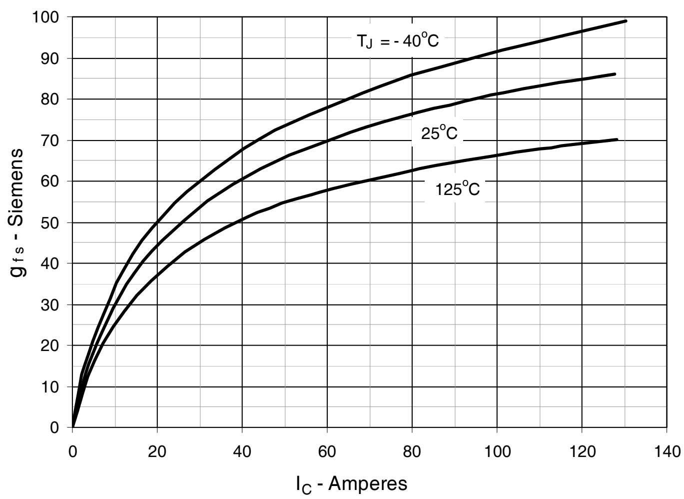


Fig. 8. Forward Voltage Drop of Intrinsic Diode

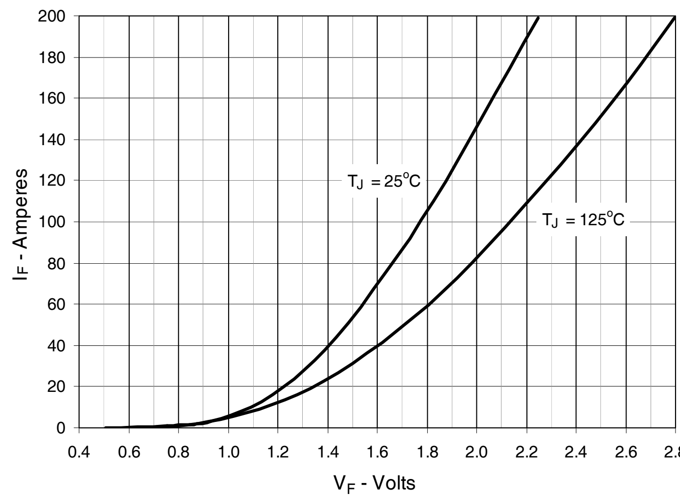


Fig. 9. Gate Charge

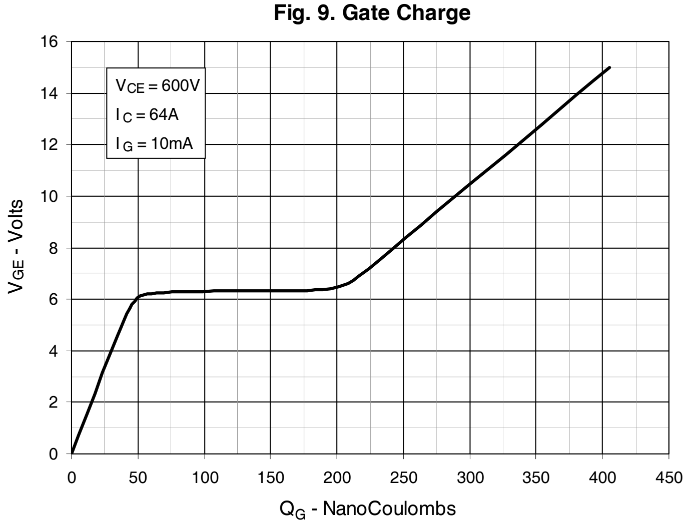


Fig. 10. Capacitance

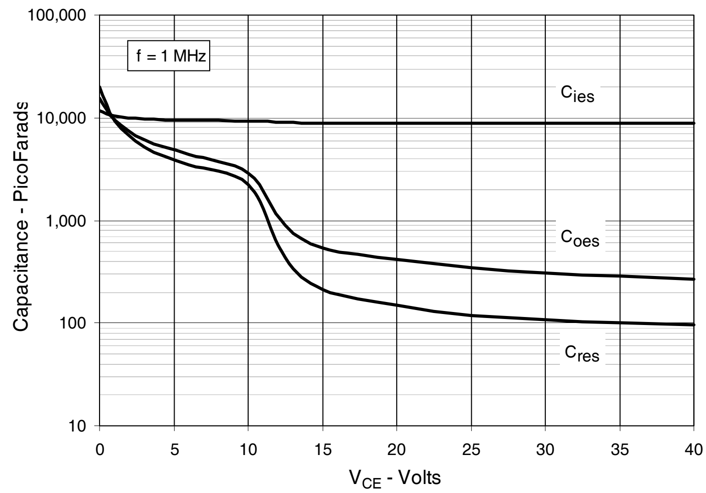


Fig. 11. Reverse-Bias Safe Operating Area

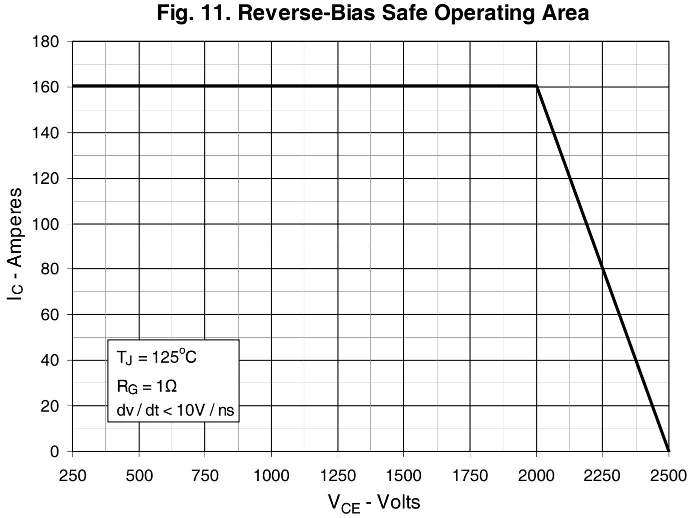


Fig. 12. Maximum Transient Thermal Impedance

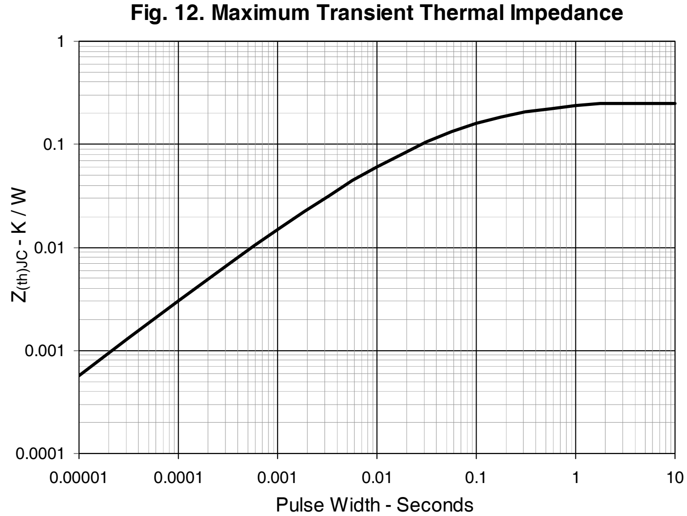


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

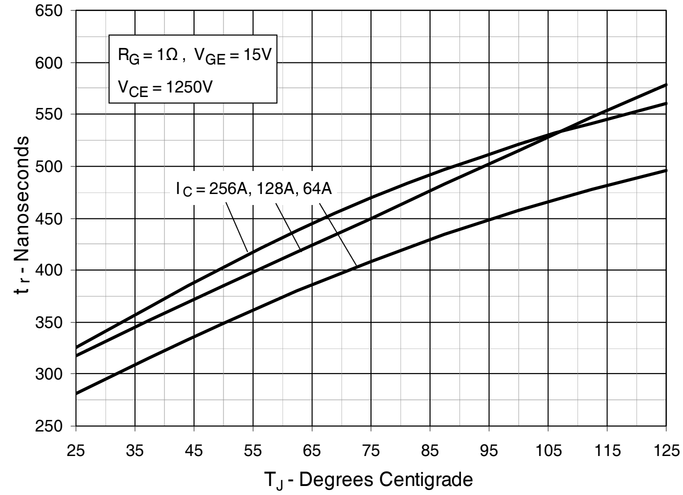


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

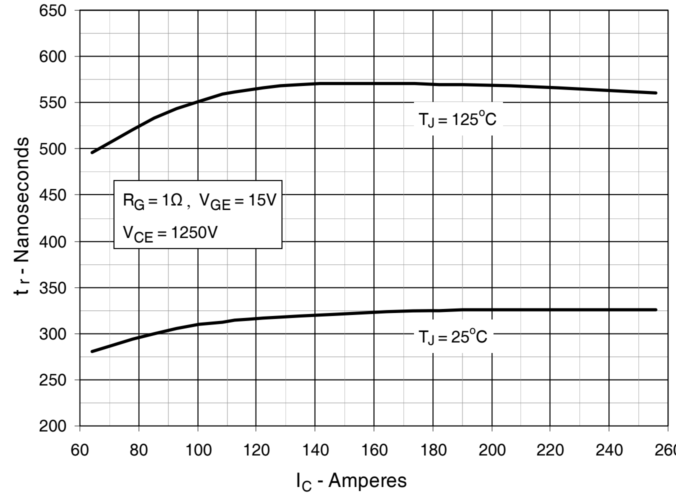


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

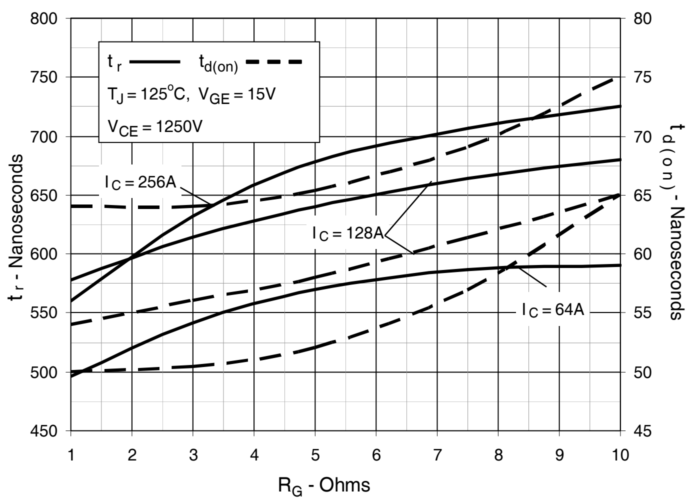


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

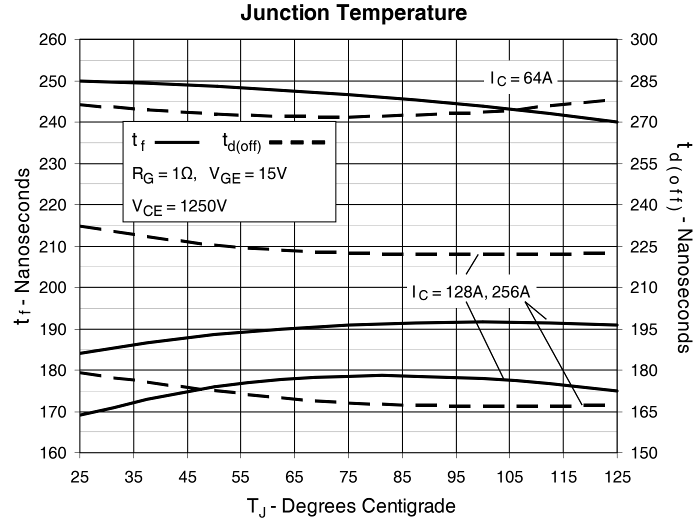


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

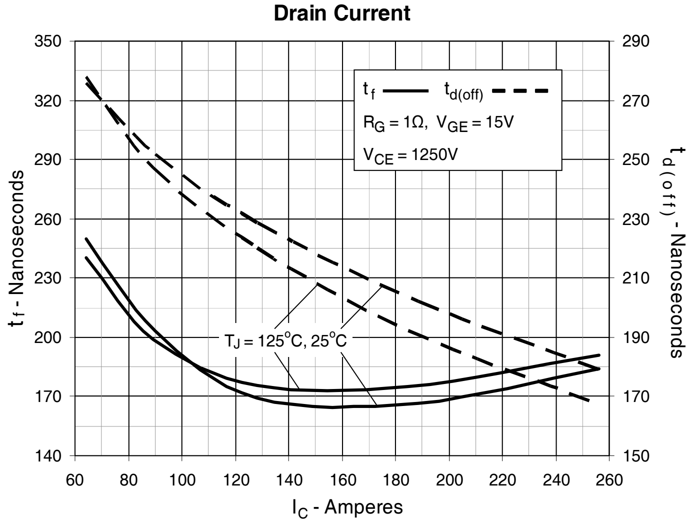


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance