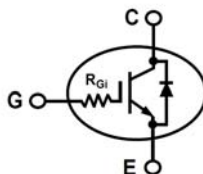


High Voltage, High Frequency, BiMOSFET™ Monolithic Bipolar MOS Transistor

IXBL60N360

(Electrically Isolated Tab)

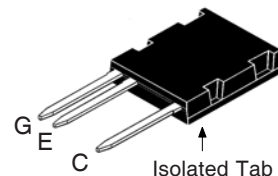


$$V_{CES} = 3600V$$

$$I_{C110} = 36A$$

$$V_{CE(sat)} \leq 3.4V$$

ISOPLUS i5-Pak™



G = Gate C = Collector
E = Emitter

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ C$ to $150^\circ C$	3600	V
V_{CGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GE} = 1M\Omega$	3600	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ C$	92	A
I_{C110}	$T_C = 110^\circ C$	36	A
I_{CM}	$T_C = 25^\circ C$, 1ms	720	A
SSOA (RBSOA)	$V_{GE} = 15V$, $T_{VJ} = 125^\circ C$, $R_G = 4.7\Omega$ Clamped Inductive Load	$I_{CM} = 480$	A
		$V_{CES} \leq 1500$	V
T_{SC} (SCSOA)	$V_{GE} = 15V$, $T_J = 125^\circ C$, $R_G = 52\Omega$, $V_{CE} = 1500V$, Non-Repetitive	10	μs
P_C	$T_C = 25^\circ C$	417	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	Plastic Body for 10s	260	$^\circ C$
F_C	Mounting Force with Clip	30..170 / 7..36	N/lb
V_{ISOL}	50/60Hz, 5 Seconds	4000	V~
Weight		8	g

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- High Blocking Voltage
- High Frequency Operation

Advantages

- Low Gate Drive Requirement
- High Power Density

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Uninterruptible Power Supplies (UPS)
- Laser Generators
- Capacitor Discharge Circuits
- AC Switches

Symbol	Test Conditions ($T_J = 25^\circ C$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$	3600		V
$V_{GE(th)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = 3000V$, $V_{GE} = 0V$ Note 2, $T_J = 100^\circ C$		125	25 μA μA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 200 nA
$V_{CE(SAT)}$	$I_C = 60A$, $V_{GE} = 15V$, Note 1 $T_J = 125^\circ C$		2.8	3.4 V
			3.4	V

Symbol Test Conditions

($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Characteristic Values

Min. Typ. Max.

g_{fs}	$I_C = 60\text{A}, V_{CE} = 10\text{V}, \text{Note 1}$	37	62	S
C_{ies}	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$		8140	pF
C_{oes}			367	pF
C_{res}			174	pF
R_{Gi}	Integrated Gate Input Resistance		5.0	Ω
$Q_{g(on)}$	$I_C = 60\text{A}, V_{GE} = 15\text{V}, V_{CE} = 1000\text{V}$		450	nC
Q_{ge}			52	nC
Q_{gc}			187	nC
$t_{d(on)}$	Resistive load, $T_J = 25^\circ\text{C}$ $I_C = 60\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 960\text{V}, R_G = 4.7\Omega$		50	ns
t_r			300	ns
$t_{d(off)}$			340	ns
t_f			910	ns
$t_{d(on)}$	Resistive load, $T_J = 125^\circ\text{C}$ $I_C = 60\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 960\text{V}, R_G = 4.7\Omega$		56	ns
t_r			674	ns
$t_{d(off)}$			370	ns
t_f			1025	ns
R_{thJC}				0.30°C/W
R_{thCS}		0.15		$^\circ\text{C/W}$

Reverse Diode

Symbol Test Conditions

($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Characteristic Values

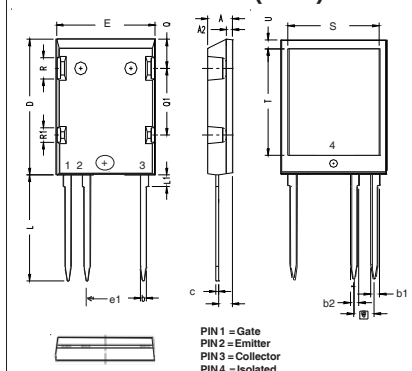
Min. Typ. Max

V_F	$I_F = 60\text{A}, V_{GE} = 0\text{V}, \text{Note 1}$		5.0	V
t_{rr}	$I_F = 30\text{A}, V_{GE} = 0\text{V}, -di_F/dt = 150\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GE} = 0\text{V}$		1.95	μs
I_{RM}			78	A
Q_{RM}			75.7	μC

Notes:

1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.
2. Device must be heatsunk for high-temperature leakage current measurements to avoid thermal runaway.

ISOPLUS i5-Pak™ HV (IXBL) Outline



SYM	INCHES		MILLIMETER	
	MIN	MAX	MIN	MAX
A	0.190	0.205	4.83	5.21
A1	0.102	0.118	2.59	3.00
A2	0.046	0.055	1.17	1.40
b	0.045	0.055	1.14	1.40
b1	0.063	0.072	1.60	1.83
b2	0.058	0.068	1.47	1.73
c	0.020	0.029	0.51	0.74
D	1.020	1.040	25.91	26.42
E	0.770	0.799	19.56	20.29
e	0.150 BSC 3.81 BSC			
e1	0.450 BSC 11.43 BSC			
L	0.780	0.820	19.81	20.83
L1	0.080	0.102	2.03	2.59
Q	0.210	0.235	5.33	5.97
Q1	0.490	0.513	12.45	13.03
R	0.150	0.180	3.81	4.57
R1	0.100	0.130	2.54	3.30
S	0.668	0.690	16.97	17.53
T	0.801	0.821	20.34	20.85
U	0.065	0.080	1.65	2.03

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

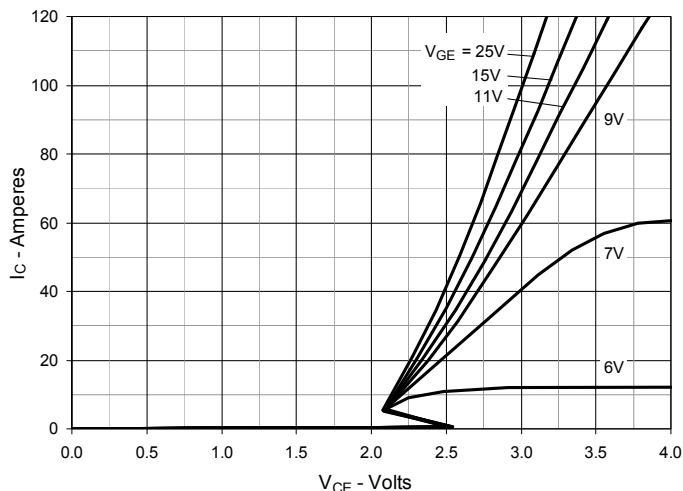
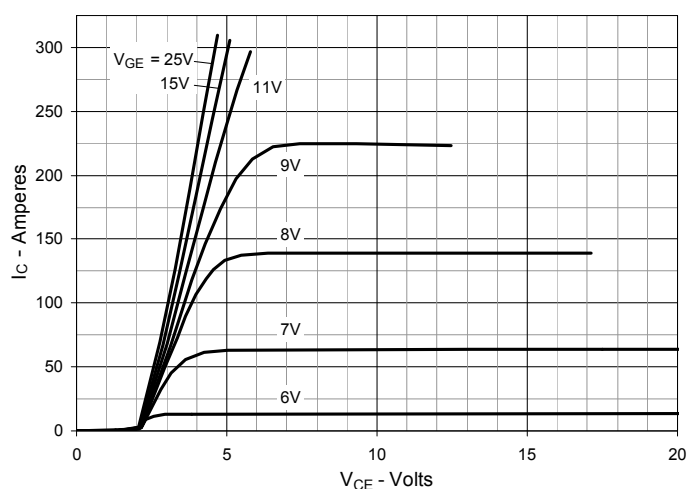
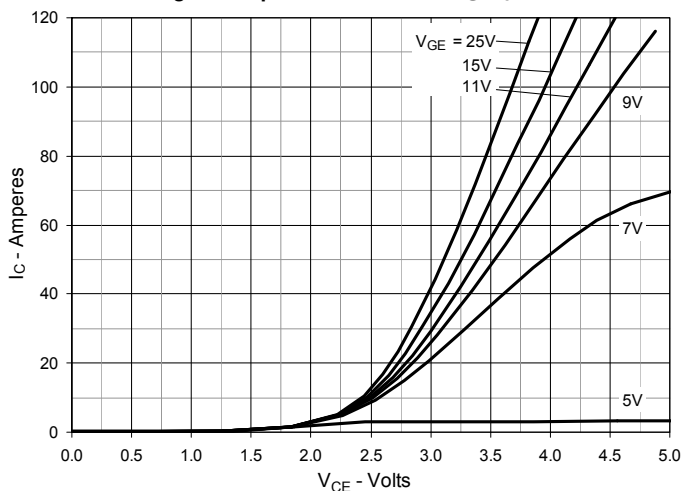
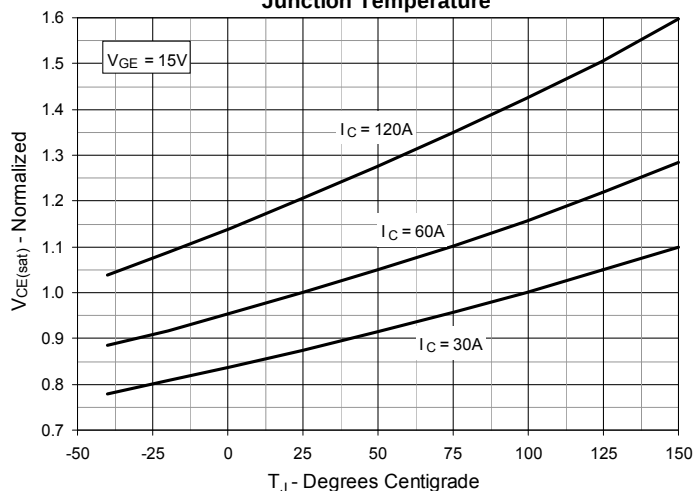
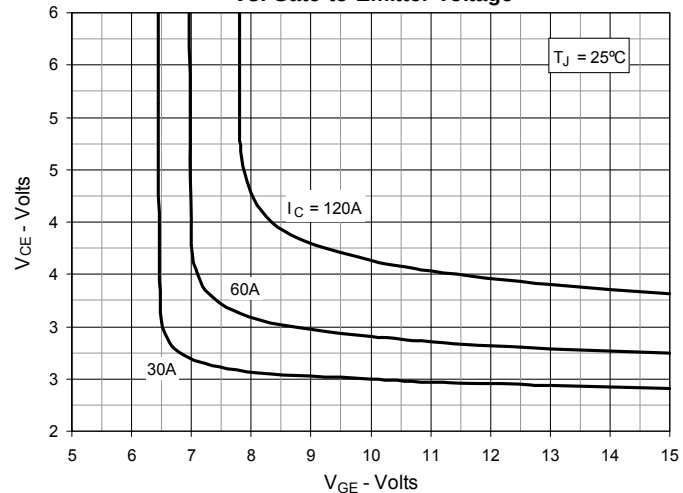
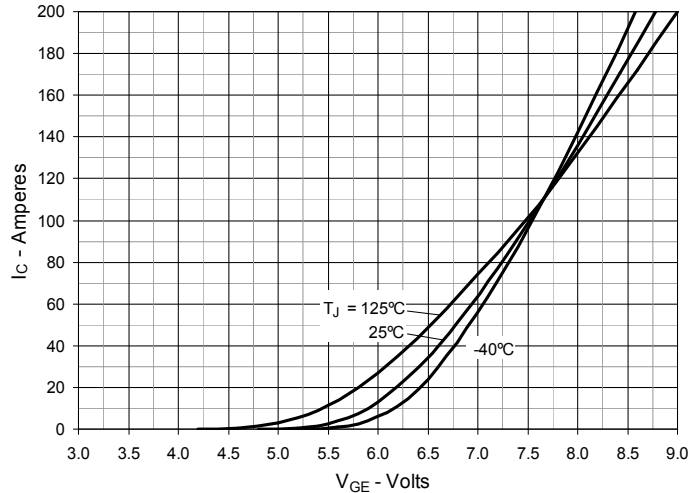
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

Fig. 6. Input Admittance


Fig. 7. Transconductance

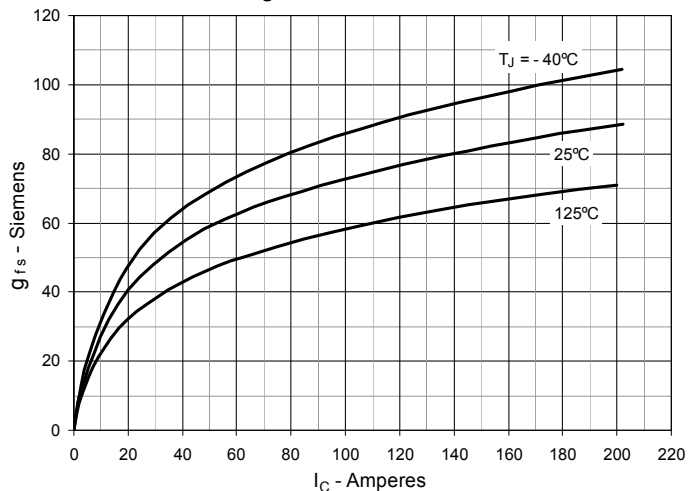


Fig. 8. Gate Charge

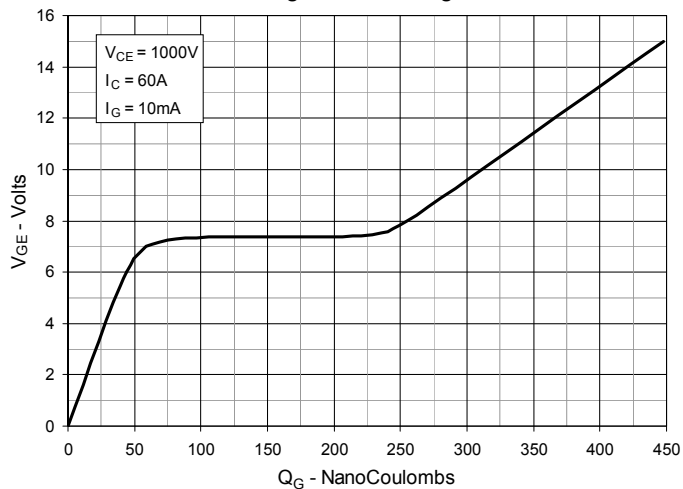


Fig. 9. Forward Voltage Drop of Intrinsic Diode

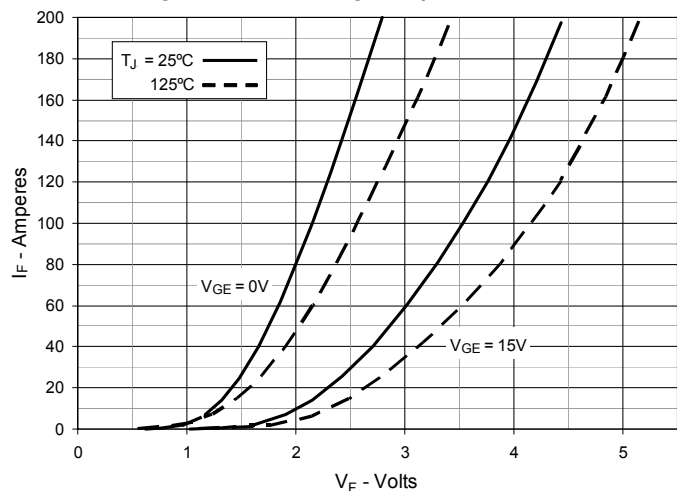


Fig. 10. Capacitance

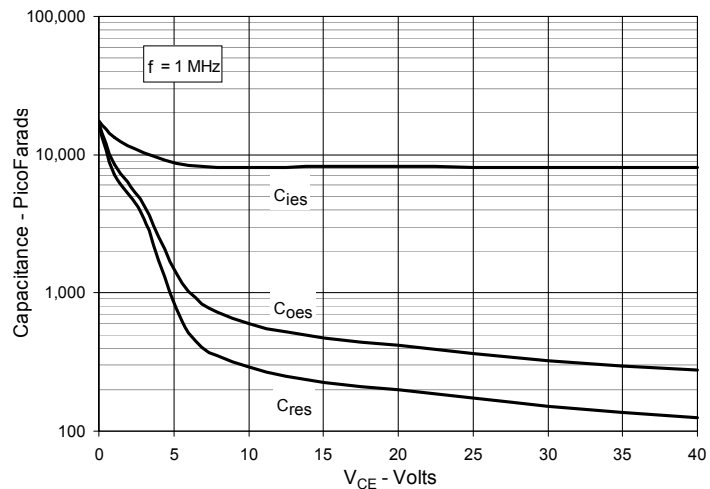


Fig. 11. Reverse-Bias Safe Operating Area

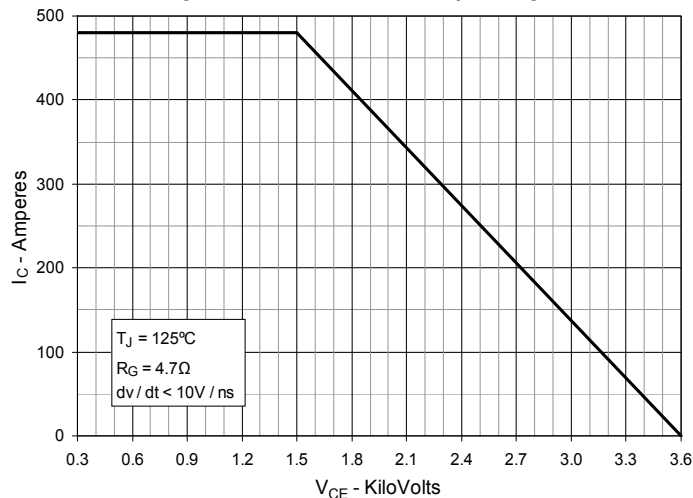


Fig. 12. Maximum Transient Thermal Impedance

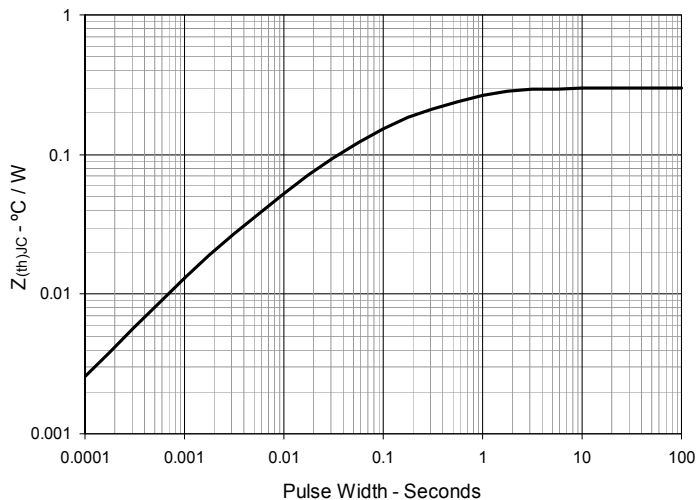
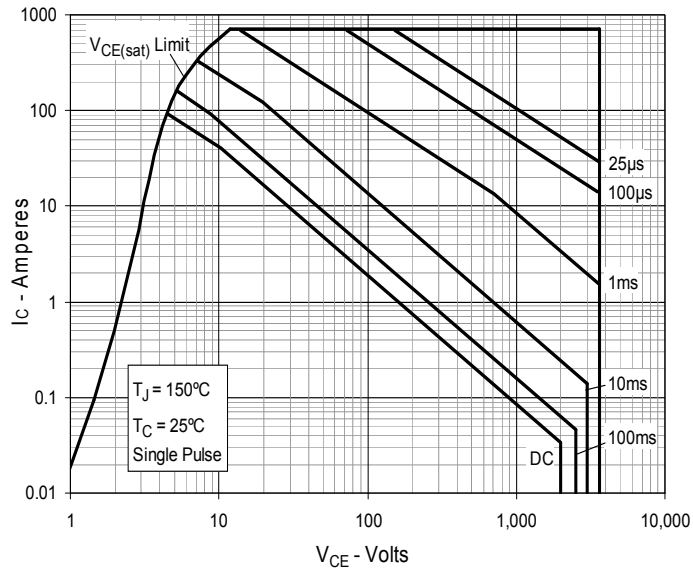
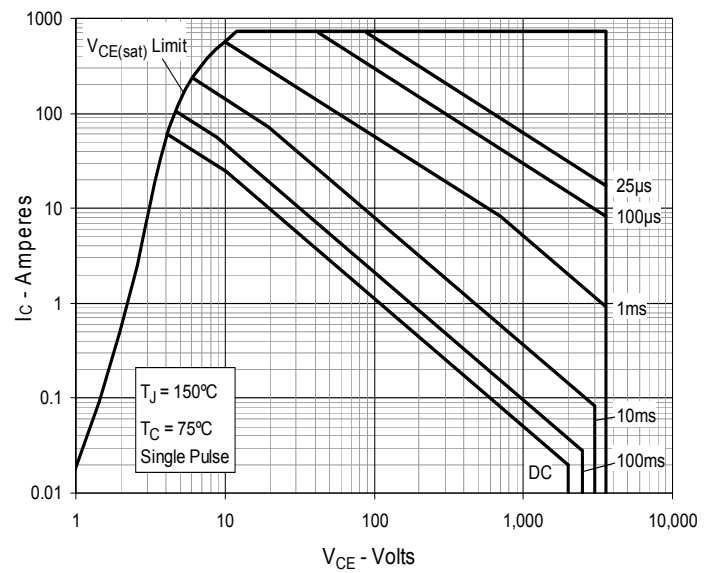


Fig. 13. Forward-Bias Safe Operating Area @ $T_C = 25^\circ\text{C}$

Fig. 14. Forward-Bias Safe Operating Area @ $T_C = 75^\circ\text{C}$




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